
603 e IMPLEMENTATION

Ref : 002581A

Duration : 4 days

OBJECTIVES

- Optimized code writing based on pipeline knowledge
- This course focuses on assembly programming and EABI understanding
- Alignment rules are to be determined to avoid cache replacement of data being processed
- Data flows between SDRAM and L1 caches are highlighted
- Cache coherency protocol is introduced in increasing depth
- This course explains 60X bus operation

RELATED COURSES

- C language for real-time and embedded applications (course 002603A)

PARTNERS

- This training course is approved by Freescale and IBM

PREREQUISITES

- Experience of a 32 bit processor or DSP is recommended

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Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS**603e PIPELINE**

- Pipeline basics
- 603e pipeline implementation
- Execution model
- Execution serialization
- Branch management : static prediction
- Guarded memory

L1 CACHES

- Cache basics
- Cache related page / block attributes
- 603e L1 cache
- Software L1 data cache flush
- Cache coherency basics
- The MEI 3-bit L1 data line state
- MEI snooping sequences involving a 603e and a PCI master

INTERNAL DATA FLOWS

- The interface buffers
- The BIU [Bus Interface Unit]
- Sync and eieio instructions

603e SPECIFIC UNITS

- The 3 architecture layers introduction : UISA, VEA and OEA
- Low power modes
- JTAG debugger, hardware breakpoint vs software breakpoints
- Real time trace building using a logic analyser, the WindRiver solution

THE UISA LAYER

- Branch instructions
- Integer load / store instructions
- Integer arithmetic and logic instructions

DOCUMENTATION

- Training manuals will be given to attendees during training in print.

- IEEE754 basics
- Float load / store instructions
- Float arithmetic instructions
- The EABI
- Code and data sections, small data areas benefits

THE VEA LAYER

- WIMG attribute bits
- Cache related instructions
- PowerPC timers : TB and DEC

THE OEA LAYER - MMU

- MMU goals
- The PowerPC address processing
- WIMG attributes definition
- Process protection through VSID selection
- TLB organization
- Page translation
- MMU implementation in real-time sensitive applications

THE OEA LAYER – EXCEPTION MECHANISM

- Exception state saving and restoring through SRR0/SRR1 registers
- Exception management : handler table, MSR update, automatic interrupt masking
- Recoverable vs non recoverable interrupts
- Requirements to support exception nesting

603e HARDWARE IMPLEMENTATION

- Bus features : address pipelining, split transactions
- 60X bus mode : address phase and data phase
- Data streaming mode
- Cache coherency protocol hardware implementation
- Other signals : interrupts, machine check