

---

## MPC7400/7410 IMPLEMENTATION

Ref : 002586A

Duration : 4 days

---

### OBJECTIVES

- Optimized code writing based on pipeline knowledge
- Alignment rules are to be determined to avoid cache replacement of data being processed
- Data flows between SDRAM, L1 caches and L2 cache are highlighted
- Cache coherency protocol is introduced in increasing depth
- Vector instructions and new C operators are viewed in detail
- Data streams parametrizing is emphasized through an example
- This course covers bus operation, either 60X or MPX mode
- Through a FFT algorithm, the instructor shows how to vectorize processing and reduce execution time using data streaming
- The internal performance monitor has been programmed so that different versions of the FFT algorithm implementation can be compared

### RELATED COURSES

- C language for real-time and embedded applications (course 002603A)

### PREREQUISITES

- Experience of a 32 bit processor or DSP is recommended

### PARTNERS

- This training course is approved by FREESCALE



### Contact

Tel : 05 62 13 52 32  
Fax : 05 61 06 72 60  
training@mvd-fpga.com

Course also available  
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

---

### TOPICS

#### MPC7400/10 PIPELINE

- Superscalar out-of-order execution
- Branch Target Instruction Cache
- Static vs dynamic branch prediction
- Coding guidelines

#### L1 AND L2 CACHES

- Cache basics
- PLRU L1 replacement algorithm, FIFO L2 replacement algorithm
- Hardware data cache flush
- Cache coherency based on snooping, the MEI, MESI and MERSI state machines

#### INTERNAL DATA FLOWS

- Data and instructions queuing mechanism to decouple bus operation and internal activity
- The Memory Sub System
- The load fold queue and the store miss merging

#### MPC7400/10 SPECIFIC UNITS

- Power management
- Performance monitor
- JTAG debugger
- Differences between 7400 and 7410

#### THE UISA LAYER]

- User registers
- Branch instructions
- Integer instructions
- IEEE754 floating point standard
- Float instructions
- EABI introduction

### DOCUMENTATION

- Training manuals will be given to attendees during training in print.

#### THE VEA LAYER]

- Cache related instructions
- Little-endian emulation
- PowerPC timers

#### ALTIVEC IMPLEMENTATION

- AltiVec registers
- Vector load / store instructions
- Vector integer instructions
- Vector float instructions
- Vector permut instructions
- ANSI C extensions to support vectors
- AltiVec implementation on 7400/10
- Data streams

#### THE OEA LAYER - MMU

- MMU goals
- Process protection
- Tablesearch, hash value
- MMU implementation in real-time sensitive applications

#### THE OEA LAYER – EXCEPTION MECHANISM

- Supervisor registers
- Context saving through SRR0/SRR1 registers
- Handler table
- Exception nesting

#### MPC7400 HARDWARE IMPLEMENTATION

- Auto-check on power up
- Bus features : address pipelining, split transactions
- 60X bus cycles
- MPX data only transactions
- Synchronous SRAM technologies
- L2 bus interface