MPC744X/745X IMPLEMENTATION

Ref : 002587A **Duration : 4 days**

OBJECTIVES

- Optimized code writing based on pipeline knowledge
- Alignment rules are to be determined to avoid cache replacement of data being processed
- Data flows between SDRAM, L1 caches , L2 and L3 cache are highlighted
- MESI cache coherency protocol is introduced in increasing depth
- Vector instructions and new C operators are viewed in detail
- Data streams parametring is emphasized through an example
- This course covers bus operation in either 60X or MPX mode
- Through a FIR algorithm, the instructor shows how to vectorize processing and reduce execution time using data streaming
- The internal performance monitor has been programmed so that different versions of the FIR algorithm implementation can be compared

RELATED COURSES

- C language for real-time and embedded applications (course 002603A)

PARTNERS

This training course is approved by FREESCALE

PREREQUISITES

- Experience of a 32 bit processor or DSP is recommended

Contact

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Course also available customized

Next sessions, see : *http://www.mvd-fpga.com/en/formationsCalend.html*

TOPICS

PIPELINE

- Pipeline basics
- 744X/5X pipeline implementation
- Issue queue resource requirements
- Execution model
- Dispatch conditions, completion conditions
- Execution serialization
- Branch management
- Guarded memory

L1, L2 and L3 CACHES

- Cache basics
- 744X/5X L1 cache
- Transient load instructions benefits
- L2 cache organization
- L2 replacement algorithm selection, L2 locking
- L3 Cache organization according to L3 size
- L2 replacement algorithm selection, L3 locking
- L3 SSRAM used as private memory
- Cache coherency basics
- The MESI L1 data line states
- MESI snooping sequences involving 2 G4 and a PCI master

INTERNAL DATA FLOWS

- L1 and L2 cache loading, hit under miss
- The MSS [Memory Sub System]
- The load fold queue
- The store miss merging advantage
- Purpose of sync and eieio instructions

MPC744X/5X SPECIFIC UNITS

- The 3 architecture layers introduction : UISA, VEA and OEA
- Low power modes
- Performance monitor
- JTAG debugger
- Real time trace
- Differences between 7441, 7445, 7450, 7451, 7455, 7447, 7457 and 7448

THE UISA LAYER

- Branch instructions
- Integer load / store instructions
- Integer arithmetic and logic instructions
- IEEE754 basics, Float load / store, and arithmetic instructions
- The EABI

THE VEA LAYER

- Cache related instructions
- Little-endian emulation
- PowerPC timers : TB and DEC

ALTIVEC IMPLEMENTATION

- Altivec introduction, SIMD processing
- Intra vs inter element instructions
- Altivec registers
- ANSI C extension to support vector operators
- Vector load / store, integer, float and Vector permut instructions
- Altivec implementation on the 744X/5X
- Data streams management
- EABI extension to support Altivec

THE OEA LAYER - MMU

- MMU goals
- The PowerPC address processing
- Enabling of 4 additional BAT on 7445/55
- 32-bit or 36-bit real address size selection
- WIMG attributes definition, page and block access rights definition
- Process protection through VSID selection
- TLB organization, Page translation
- Software vs hardware TLB reload
- MMU implementation in real-time sensitive applications

THE OEA LAYER – EXCEPTION MECHANISM

- Exception management
- Registers updating related to the exception cause
- Requirements to support exception nesting

MPC744X/5X HARDWARE IMPLEMENTATION

- Bus interface configuration
- Auto-check on power up
- Pinout
- Bus features : address pipelining, split transactions
- 60X bus mode : address phase and data phase
- MPX bus mode : *HIT and *DRDY pins use
- Data only transactions
- MPX bus cycles overview
- Other signals : interrupts, machine check
- Synchronous SRAMs technologies
- L3 bus pinout, L3 clock synchronization
- SSRAM related parameters initialization in L3CR register

DOCUMENTATION

- Training manuals will be given to attendees during training in print.