

MPC 8XX IMPLEMENTATION

Ref : 002590A

Duration : 5 days

OBJECTIVES

- PowerPC core low level programming
- MMU Translation Lookaside Buffers loading from a table containing the page features
- GPCM and UPMs state machines initializing to support FLASH, SRAM, DRAM and SDRAM
- SIRAM programming to handle RNIS frames
- Generic interrupt handler development
- Ethernet controller configuring in promiscuous mode
- HDLC multi-channel implementation
- Fast Ethernet controller auto-negotiation understanding
- Debug capabilities and real time trace requirements

RELATED COURSES

- C language for real time embedded applications (002603A)

PREREQUISITES

- Experience of a 16/32 bit processor or DSP is recommended

PARTNERS

- This training course is approved by FREESCALE


WIND RIVER

NeoMore

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Course also available
 customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

MPC8XX INTRODUCTION

- MPC8XX block diagram : the PowerPC core, SIU and CPM modules
- The 3 registers families : GPRs, SPRs, and memory-mapped
- The 860 derivatives features : 85X, 86X, 87X and 88X
- Performance estimation

PowerPC CORE ARCHITECTURE

- RCPU pipeline, history buffer, isync instruction
- Execution units
- Cache basics
- Load/store architecture
- Sync and eieio instructions

PowerPC CORE PROGRAMMING

- User registers
- Branch, Integer load / store and Integer arithmetic instructions
- The EABI, Code and data sections
- Cache related instruction
- Exception management at core level : handler table, priority
- MMU basics, Tablewalk through the descriptor tables description
- TLB entry software loading

THE SYSTEM INTERFACE UNIT

- The interrupt controller
- MPC8XX hardware configuration word at reset
- Clock synthesizer

THE EXTERNAL BUS INTERFACE

- Dynamic bus sizing, connection of 8 and 16-bit peripherals
- Single data read and write timing diagrams
- Burst read and write timing diagrams
- Shared resource control, Bus error, retry

THE MEMORY CONTROLLER

- Address decoding through BR/OR registers
- GPCM timing parameters explanation
- SDRAM basics, Connection of an SDRAM, UPM initialization

CPM BASICS

- Synchronization between RCPU and CP through the Command Register
- DPRAM organization
- The CPM Interrupt Controller
- CPM general purpose timers
- IDMA channels
- General purpose IO : pin configuration

THE SERIAL INTERFACE

- ISDN basics, NMSI vs TDM
- SIRAM initialization to support ISDN frames

DOCUMENTATION

- Training manuals will be given to attendees during training in print.

- Transmit and Receive clock selection from the bank of clocks
- Buffer Descriptor rings allocation
- Buffer chaining, Transmit and receive interrupts

THE SERIAL MANAGEMENT CONTROLLERS

- Supported protocols : transparent, UART and auxiliary ISDN channel
- SMC in UART mode
- SMC restrictions compared to SCC
- Initialization sequence : registers, Parameter RAM, Buffer Descriptors

THE SERIAL COMMUNICATION CONTROLLERS

- The DPLLs : clock recovery
- UART, HDLC and Ethernet on SCC : 7-wire interface with the transceiver
- Hash table restrictions, External CAM connection

THE SPI CONTROLLER

- SPI protocol, Clock polarity and phase selection
- Transmit and receive sequences

THE I2C CONTROLLER

- I2C basics, Read and Write sequences
- Upload of SDRAM parameters located in a DIMM serial EEPROM

THE USB CONTROLLER

- USB protocol basics
- MPC885 USB controller features
- Hardware interface, Architecture, Programming model
- Initialization sequence, Read and Write sequences

THE FAST ETHERNET CONTROLLER

- CPM independence, MII pinout, 7-wire vs MII transceiver connection
- Buffer descriptor description
- Initialization sequence

THE MULTI CHANNEL CONTROLLER

- Logic channel vs time slot, The time slot assignment tables
- Logic channel processing
- Interrupt queues
- Parameterizing the interface to the framer

THE SECURITY ENGINE

- Encryption basics, SEC features
- Memory mapping and programming interface
- Crypto channel management
- Master/Slave interface module description
- Initialisation sequence

THE DEBUG PORT

- BDM features : watchpoints and breakpoint, Programming interface
- BDM restrictions, Real time trace solution