
COLDFIRE 5X07 IMPLEMENTATION

Ref : 002592A

Duration : 4 days

OBJECTIVES

- The course describes the ColdFire assembly language and highlights differences from 68K instructions
- An example of SDRAM controller initialization is provided
- Interfacing with external devices is explained
- The interrupt controller is viewed in detail
- Interrupt driven DMA transfers are studied
- A programming example has been developed for each internal peripheral (serial; I2C, timer)

RELATED COURSES

- The training course called "C language for real time and embedded applications" could be useful for low level programming developers. This training has the reference 002603A.

PREREQUISITES

- Experience of a 32 bit processor or DSP is mandatory

PARTNERS

- This training course is approved by FREESCALE



Contact

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Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

5307 INTRODUCTION

- Coldfire roadmap
- Differences between ColdFires and 68K processors
- 5307 block diagram
- Memory mapped I/O organization

V3 CORE

- 5307 pipeline
- Programming model
- Addressing modes
- Instruction set
- Stack management, subroutine call and return
- C to assembly interface
- Exception management
- Internal SRAM
- 5307 cache operation

HARDWARE IMPLEMENTATION

- Dynamic bus sizing
- Address decoding
- Arbitration
- Burst cycles
- Bus error management

DEBUG FACILITIES

- Intrusive vs non-intrusive debug
- BDM port
- Hardware breakpoints
- Trace port

THE SIM MODULE

- The interrupt controller
- The software watchdog
- Reset, self-configuration
- Clock synthesis
- General Purpose I/O pins

THE MEMORY CONTROLLER AND THE DRAM/SDRAM CONTROLLER

- SRAM connection, chip-select programming
- DRAM / SDRAM basics
- The 5x07 (S)DRAM controller : address decoding, refresh rate definition, address multiplexing selection

THE SERIAL PORTS

- Asynchronous ports
- Transmit and receive sequences
- Synchronous port : I2C basics
- Transmit and receive sequences

THE DMA CONTROLLER

- Single address vs dual address transfers
- Hardware interface, hardware initiated transfers
- Programming model

THE TIMERS

- Capture mode
- Period selection
- Interrupt control

5407 ENHANCEMENTS

- V4 core enhancements
- Instruction set additions
- Enhanced memories
- On-chip DMA and serial ports modifications

DOCUMENTATION

Training manuals will be given to attendees during training **both in pdf and in print**. Precise and easy to use, those notes can be used as a reference afterwards.

CONTACT INFORMATIONS

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