

HCS 12 IMPLEMENTATION

Ref : 002593A

Duration : 3 days

OBJECTIVES

- The course explains how to design a HCS12 based board
- BDM debug port is described
- A generic interrupt handler written in C language has been developed
- The course details the C-to-assembly interface
- The course focusses on internal IOs, and for each of them a C programming example is provided

RELATED COURSES

- OSEK implementation (002604A)
- CAN bus (reference 002601A)
- C for real-time and embedded applications (course 002603A)

PARTNERS

- This training course is approved by FREESCALE

PREREQUISITES

- Basic knowledge about processors

**WIND RIVER****NeoMore**

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Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

HCS12 MICROCONTROLLER FAMILY INTRODUCTION

- HCS12 microcontrollers architecture
- Differences between HC12 and HCS12 families

THE STAR12 CORE

- The instruction pipeline
- Branch instructions
- Addressing modes
- Arithmetic and logic instructions
- Bit instructions, shift and rotate instructions
- Mac instructions
- Interpolate instructions
- Stack management
- C-to-assembly interface
- Low power modes

EXCEPTION MANAGEMENT

- Exception management sequence
- Vectorization
- Exception priority
- Reset

DEBUG FACILITIES

- Hardware vs software breakpoints
- BDM protocol
- Securing the microcontroller

SYSTEM ON CHIP APPROACH

- Core interface signals
- External bus signals
- Clock and reset generator module
- PLL operation
- Core wake up

THE SIM MODULE

- Chip select programming
- Internal RAM and EEPROM base address selection
- Input / output parallel port configuration

MC9S12DP256B HARDWARE IMPLEMENTATION

- Signal descriptions
- Bus operation
- Timing diagrams

DOCUMENTATION

- Training manuals will be given to attendees during training in print.

THE FEPROM

- Erase sequence
- Program sequence
- Test mode

THE EEPROM

- Erase and program clock selection
- Byte, page or block erase
- Program sequence

THE INTERRUPT CONTROLLER AND THE SYSTEM TIMERS

- Vector table description
- The COP
- The real time interrupt

THE ENHANCED CAPTURE TIMER MODULE

- Capture inputs
- Compare outputs
- Pulse accumulators

THE PWM GENERATORS

- Period and duty cycle selection
- Left or center aligned output modes

THE COMMUNICATION CONTROLLERS

- SPI controller : master vs slave selection
- Polarity selection
- UART controller
- Bit rate selection
- Point to multipoint communication : receiver wake up modes
- I2C Timing diagrams
- Transmit and receive sequences
- The MSCAN controllers
- Message buffers structure
- Timing and synchronization
- Error management
- Low power modes

THE ADC

- Analog inputs multiplexing
- Conversion timing
- External trigger use