# DSP56F83XX Family

**Course description (ref. 002594A)** **Duration: 3 days**

## OBJECTIVES

- Give to the project manager an in depth presentation to be able to use efficiency all the resources of the component
- Give to the developer a good understanding to set up easily all the internal functions
- Optimized coding examples are described
- A generic interrupt handler is introduced
- Practical exercices are executed on a 56F8323 simulator using Codewarrior and Processor Expert tools

## RELATED COURSES

- CAN bus training (ref. 002601A)
- C language for real-time and embedded applications (ref 002603A)

## PREREQUISITES

- Experience of a microcontroller is recommended
- This training is adapted to the electronics and programmers engineers confronted with the problems of the implementation of this processor

## PARTNERS

- This training course is approved by Freescale

freescale™ Alliance Member

WIND RIVER

LAUTERBACH DEVELOPMENT TOOLS


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**Course also available customized**

**Next sessions, see: *http://www.mvd-training.com/en/schedule.html***

## TOPICS

### INTRODUCTION TO DIGITAL SIGNAL PROCESSING

- Arithmetic processing of real-time signals
- Filtering, convolution, correlation
- Modified dual Harvard architecture
- DSP 56F83xx family introduction

### 56F83XX ARCHITECTURE

- Core busses
- Processing states
- Reset, low voltage, stop and wait operations
- Mapping

### THE DSP CORE

- The Data ALU
- The Address Generation Unit
- The Program Control Unit
- The instruction set
- C-to-assembly interface
- Software techniques
- Exception management
- The interrupt routing performed by the ICTN
- The debugging support
- JTAG use to access the OnCE
- The embedded flash memory
- Program sequence
- Erase sequence

### HARDWARE IMPLEMENTATION

- On chip clock synthesis
- Wait state X data memory
- Wait state program memory

### THE QUAD TIMER MODULE

- Timer module pinout
- Operating modes
- OFLAG output signal

### THE ADCs

- Timing, pipelining
- Conversion sequence definition
- Synchronization to the PWM
- Optional sample correction

### THE QUADRATURE DECODERS

- Quadrature decoders pinout
- Configurable digital filters
- Watchdog timer implementation

### THE PULSE WIDTH MODULATORS

- Independent or complementary channel operation
- Deadtime generators
- IFault protection

### THE SCI AND THE SPI MODULES

- SCI block diagram, IO signals
- Asynchronous vs synchronous operation modes
- Baud rate selection
- Bootstrap loading from the SCI
- Asynchronous transmit and receive sequences
- SPI synchronous communications basics
- Master vs slave selection
- Polarity selection

### THE FLEXCAN CONTROLLER

- The FLEXCAN controllers
- Message buffers structure
- ID bit masking
- Arbitration
- Timing and synchronization
- Error management

### DOCUMENTATION

Training manuals will be given to attendees during training in print.