
DSP56F83XX IMPLEMENTATION

Ref : 002594A

Duration : 3 days

OBJECTIVES

- The course explains how to design a 56807 based board
- Optimized coding examples are described
- A generic interrupt handler is introduced
- The course focuses on motor driving
- Practical exercises are executed on a 56807 board

RELATED COURSES

- The **Metrowerks** compiler suite is viewed in detail in the 002608A training
- The 2-day CAN bus training (reference 002601A) is recommended for persons involved in development of a FLEXCAN driver

PREREQUISITES

- Basic knowledge about signal processing and motor control

PARTNERS

- This training course is approved by FREESCALE

PRACTICAL LABS

- Labs are executed on XXX evaluation board



Contact

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Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

INTRODUCTION TO DIGITAL SIGNAL PROCESSING

- Arithmetic processing of real-time signals
- Filtering, convolution, correlation
- Modified dual Harvard architecture
- DSP 568XX family introduction, compatibility with 5600X DSPs
- Introduction of motor types

563XX ARCHITECTURE

- Core busses
- Processing states
- Reset, low voltage, stop and wait operations
- 56807 mapping

THE DSP CORE

- The Data ALU
- The Address Generation Unit
- The Program Control Unit
- The instruction set
- C-to-assembly interface
- Software techniques
- Exception management
- The interrupt routing performed by the ICTN
- The debugging support
- JTAG use to access the OnCE
- The embedded flash memory
- Program sequence
- Erase sequence

HARDWARE IMPLEMENTATION

- On chip clock synthesis
- Wait state X data memory
- Wait state program memory

THE QUAD TIMER MODULE

- Timer module pinout
- Operating modes

- OFLAG output signal

THE ADCs

- Timing, pipelining
- Conversion sequence definition
- Synchronization to the PWM
- Optional sample correction

THE QUADRATURE DECODERS

- Quadrature decoders pinout
- Configurable digital filters
- Watchdog timer implementation

THE PULSE WIDTH MODULATORS

- Independent or complementary channel operation
- Deadtime generators
- IFault protection

THE SCI AND THE SPI MODULES

- SCI block diagram, IO signals
- Asynchronous vs synchronous operation modes
- Baud rate selection
- Bootstrap loading from the SCI
- Asynchronous transmit and receive sequences
- SPI synchronous communications basics
- Master vs slave selection
- Polarity selection

THE FLEXCAN CONTROLLER

- The FLEXCAN controllers
- Message buffers structure
- ID bit masking
- Arbitration
- Timing and synchronization
- Error management

DOCUMENTATION

Training manuals will be given to attendees during training **both in pdf and in print**. Precise and easy to use, those notes can be used as a reference afterwards.

CONTACT INFORMATIONS

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