

IEEE 1394 a/b BUS

Ref : 002600A

Duration : 4 days

OBJECTIVES

- Differential transmission advantages are highlighted
- The course explains the bus initialization process
- Packet format and subaction transactions are described with the assistance of the CATC FireInspector
- 1394a arbitration enhancements are emphasized
- The course describes the new 1394b beta signalling
- After having introduced digital camera fundamentals, isochronous traffic is analysed

RELATED COURSES

- The PCI bus training whose reference is 002596A may be interesting to understand the operation of PCI-to-1394 bridges

PREREQUISITES

- Experience of a digital bus is recommended

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Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

1394-1995 OVERVIEW

- Bus creation and history
- 1394 bus architecture
- Technical introduction : time-slicing
- Support of asynchronous and isochronous transactions
- Protocols stack

LAYER MODEL

- The transaction layer
- The link layer
- The physical layer
- The management layer

HARDWARE IMPLEMENTATION

- Data and strobes encoding
- Line states for arbitration, configuration and reset
- Decoding rules
- Idle bus delays to enable arbitration requests : the gaps
- Power Classes
- Suspend / Resume mechanism

SOFTWARE INTERFACE

- IEEE1212 address definition and node mapping
- Link layer Control & Status Registers
- Link layer configuration ROM organization
- PHY layer registers

BUS INITIALIZATION

- Reset causes
- Initialization steps
- Tree building, contention resolution
- Self-ID process, Self-ID packet format
- Software configuration
- Initializations performed by the Bus Manager

1394/1394a ARBITRATION

- Geographic priority
- Arbitration for asynchronous transfers
- Arbitration for synchronous transfers
- Inefficiency of gaps when data rate increases
- 1394a optimizations

ASYNCHRONOUS TRANSACTIONS

- Resource locking
- Cycle start packet
- Retry goals
- Single-phase retry

DOCUMENTATION

- Training manuals will be given to attendees during training in print.

- Dual-phase retry
- Transaction errors management

1394-BASED DIGITAL CAMERA SPECIFICATION

- Digital camera control command registers
- Camera initialize register
- Isochronous packet format for VGA non compressed format (Format_0)
- Video data payload structure

ISOCHRONOUS TRANSACTIONS

- Talker and listeners
- Channel number and bandwidth allocation
- Real time data flows requirements

PHY-LINK INTERFACE

- PHY register access
- Status information transmission from PHY to Link
- Packet transmission timing diagram
- Packet receipt timing diagram

1394b OVERVIEW

- New transmission media : max data rate and max distance between 2 peer nodes according to the media
- Bilingual ports

BETA SIGNALLING

- Full duplex communication
- Symbols tables
- Scrambler / Descrambler operation
- Benefits of 8B/10B encoding
- Descrambler synchronization : training sequence

1394b ARBITRATION

- Symbol use instead of gaps
- Bus requests pipelining, arbitration phases
- Arbitration in a hybrid tree including DS ports and Beta ports

CONNECTION MANAGEMENT

- Auto-negotiation
- Standby / Restore mechanism
- Loop removing

1394b PHY-LINK INTERFACE

- Enhancement of the 1394a PHY-LINK interface to support S800
- New PIL-FOP interface to support higher data rates
- Galvanic isolation
- New PHY registers description