
Tsi107 PCI BRIDGE

Ref : 002605A

Duration : 2 days

OBJECTIVES

- The course details Tsi107 internal datapaths
- The I2O synchronization mechanism is studied
- SDRAM timing parameters initialization is described
- The training explains how to use the DMA controller to transfer data from SDRAM to PCI space

RELATED COURSES

- The 60X bus is explained in PowerPC CPU trainings
 - 603e (ref 002581A)
 - 7XX (ref 002582A)
 - 7400/10 (ref 002586A)
 - 744X/5X (ref 002587A)
 - MPC826X (ref 002589A)
- PCI bus (002596A)

PREREQUISITES

- PCI knowledge and 60X bus knowledge are recommended

PARTNERS

- This training course is approved by FREESCALE



Contact

Tel : 05 62 13 52 32
Fax : 05 61 06 72 60
training@mvd-fpga.com

Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

Tsi107 OVERVIEW

- Clock generation, DLL benefits
- Memory mapping
- Explanation of the translation mechanism to access PCI MEM space
- Explanation of the translation mechanism used when PCI masters access the local SDRAM

THE SDRAM CONTROLLER

- SDRAM basics
- Mode register initialization
- Command truth table
- Tsi107 memory controller introduction
- Address multiplexing
- The Flash EPROM controller
- X-port advantages and restrictions

THE PCI INTERFACE

- Commands supported when the Tsi107 is PCI master
- Commands supported when the Tsi107 is PCI target
- Configuration space access through CONFIG_ADDRESS and CONFIG_DATA registers

THE 60X INTERFACE

- 7XX or 74XX PowerPC connection

- 60X slave connection
- Error management

THE INTERRUPT CONTROLLER

- EPIC operation modes
- Interrupt request time-multiplexing
- Interrupt nesting requirements
- Integrated timers
- Doorbell registers
- I2O specification basics, synchronization by messages

THE DMA CONTROLLER

- Direct mode vs chained buffer mode
- Programming model
- Transfer descriptor initialization when the scatter / gather mode is selected

THE I2C CONTROLLER

- I2C basics
- Interrupt driven communication sequence

RESET

- Configuration pins sampling upon reset
- Initialization sequence

DOCUMENTATION

- Training manuals will be given to attendees during training in print.