
PPC 405 CORE

Ref : 002630A

Duration : 3 days

OBJECTIVES

- A boot firmware that initializes the MMU has been developed
- Internal debug facilities are described
- OCM memory benefits compared to cache are highlighted
- The course focusses on 405 low level programming, especially the PowerPC EABI
- Examples of exception handlers are provided
- A DFT has been developed to explain how to use mac instructions

RELATED COURSES

- The knowledge of C language for real-time and embedded applications (course 002603A) is recommended
- To fully cover the Virtex-II Pro / Virtex-4 FX technology, several training modules have been developed : CoreConnect (course 002585A), Rocket IOs (course 002843A) and EDK (course 002844A)

PREREQUISITES

- Experience of a 32 bit processor or DSP is mandatory

PARTNERS

- This training course is approved by IBM Electronics

Authorized
Training Provider

Contact

Tel : 05 62 13 52 32
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training@mvd-fpga.comCourse also available
customizedNext sessions, see : <http://www.mvd-fpga.com/en/formations002630A.html>

TOPICS

INTRODUCTION TO 405

- Architecture of a 405-based System-on-Chip
- Programming model, the 4 register groups GPRs, SPRs, DCRs and memory mapped

THE CORE ARCHITECTURE

- 5-stage pipeline operation
- Instructions flows through the pipeline
- Speculative execution, guarded memory, SGR register
- Serialization : prefetch barrier implementation by means of unconditional branch instructions, isync instruction
- Cache basics : organization, replacement algorithm, write policies
- Data flow between external memory and caches
- Cache programming interface
- Memory Management Unit : memory attributes definition (cache enabled / cache inhibited, copyback / writethrough)
- Translation Lookaside Buffer initialisation
- Parity control for caches and UTLB
- Cache control and debugging features
- Load / store buffer, sync instruction

PowerPC ARCHITECTURE FOR EMBEDDED APPLICATIONS

- Branch instructions
- System call instruction
- Load / store instructions
- Semaphore management with lwarx / stwcx. Instructions
- Arithmetical and logical instructions
- The PowerPC EABI
- Cache related instructions
- 16-bit mac instructions

- Exception processing
- Critical versus non critical interrupts
- Syndrome registers updating when an exception is taken
- Core timers : PIT, FIT and WDT
- Reset

INTEGRATED DEBUG FACILITIES

- JTAG debug
- Logic analyser connection through Mictor connectors
- The 405 instruction trace port
- Hardware vs software breakpoints

HARDWARE IMPLEMENTATION OF THE PPC405 CORE

- External connections
- Clock and power management interface
- CPU control interface
- Reset interface
- External interrupt controller interface
- The OCM busses
- Instruction-side local bus interface
- Data-side local bus interface
- DCR interface

APU CONTROLLER

- Connection to the native instruction pipeline
- External coprocessor module
- Software interface
- Class of instruction
- Developing a custom instruction set relying on an external coprocessor

DOCUMENTATION

Training manuals will be given to attendees during training **both in pdf and in print**. Precise and easy to use, those notes can be used as a reference afterwards.

CONTACT INFORMATIONS

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