

Designing for performance, ISE

Ref : 002833A

Duration : 2 days

OBJECTIVES

- This course will help you to optimize your design so that it can fit into a smaller and/or slower FPGA or simply meet timing constraints.
- Understanding the development flow to meet the timing constraints.
- Use of DCMs/PLLs and other clock circuitries.
- Registers duplication and pipeline.
- Re-synchronization circuit usage.
- Use of Core Generator.
- Find and correct design bottlenecks using static timing analyzer.
- Advanced timing constraints.
- Advanced implementations options to improve performance.

PREREQUISITES

- This course is aimed at electronics engineers with intermediate knowledge in HDL language and some experience on the ISE tools.

TRAINING MATERIALS

Software Configuration :

- Xilinx ISE Design Suite 13.1 Logic Edition

Recommended Hardware Configuration :

- Intel Core 2 or more recent
- Windows XP or 7
- 1 GB Free disk after software installation
- At least 2Go RAM
- Minimum Display resolution : 1024 x 768
- On Site training : video projector

RELATED COURSES

- VHDL logical synthesis and simulation for Xilinx FPGA design (002572A)
- Advanced FPGA implementation (002834A)
- Designing with PlanAhead (004088A)

PARTNERS

- This training course is approved by XILINX

**XILINX**Authorized
Training Provider

Contact

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Course also available
customized on site

Next sessions, see : <http://www.mvd-training.com/en/schedule.html>

TOPICS

1st day

- Introduction
- FPGA resources
- Core Generator
- Basic FPGA Clock resources
- Virtex-6/Spartan-6 Clock resources
 - Lab
- FPGA design techniques
- Synthesis techniques
 - Lab

* Lab on Chipscope Pro is optional

2nd day

- Achieving Timing Closure
 - Lab : Review of global timing constraints
- Path-Specific Timing Constraints
 - Lab
- Advanced implementations options
 - Lab
- Chipscope Po Software
 - Lab *

DOCUMENTATION

Training manuals will be given to attendees during training in print.