
Advanced FPGA Implementation

Ref : 002834A

Duration : 2 days

OBJECTIVES

- Who Should Attend ?
Engineers who seek advanced training in using Xilinx tools to improve FPGA performance and utilization while also increasing productivity
- This training course covers the most advanced ISE suite tools and Xilinx hardware.
- Implement designs via the Tcl command line
- Timing constraints in the UCF file
- IOs Timing constraints in system-synchronous and source-synchronous.
- SmartGuide technologies
- Use the PlanAhead™ tool to create area constraints
- FPGA Editor using

RELATED COURSES

- Designing for performance, ISE (002833A)
- VHDL logical synthesis and simulation for Xilinx FPGA design (002572A)

PARTNERS

- This training course is approved by XILINX

PREREQUISITES

- At least six months of design experience with Xilinx tools and FPGAs
- Designing for performance (002833A) course completed
- Xilinx FPGAs architectures knowledge
- Intermediate knowledge of an HDL language

TRAINING MATERIALS

Software Configuration :

- Xilinx ISE Design Suite 11.3 Logic Edition

Recommended Hardware Configuration :

- Intel Core 2 or equivalent
- Windows XP
- 1 GB Free disk after software installation
- At least 1Go RAM
- Minimum Display resolution : 1024 x 768
- On Site training : video projector



Contact

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Course also available
customized

Next sessions, see : <http://www.mvd-training.com/en/schedule.html>

TOPICS

1st day

- Introduction
 - Exercise : Review of timing constraints
- UCF file editing and syntax
 - Exercise
- Advanced IO timing Constraints
 - Exercise
- TCL Script

2nd day

- Exercise
- SmartGuideTechnology
 - Exercise
- Area Placement (Floorplanning)
 - Exercise
- FPGA Editor
 - Exercise : routing editing (ILA, Probing)

DOCUMENTATION

Training manuals will be given to attendees during training in print.