
Advanced FPGA Implementation

Ref : 002834A

Duration : 2 days

OBJECTIVES

- Who Should Attend ?
Engineers who seek advanced training in using Xilinx tools to improve FPGA performance and utilization while also increasing productivity
- This training course covers the most advanced ISE suite tools and Xilinx hardware.
- Implement designs via the Tcl command line
- Timing constraints in the UCF file
- IOs Timing constraints in system-synchronous and source-synchronous.
- Use the PlanAhead™ tool to create area constraints
- SmartGuide technologies and Partitions
- FPGA Editor using

RELATED COURSES

- VHDL logical synthesis and simulation for Xilinx FPGA design (002572A)
- Designing for performance, ISE (002833A)
- Designing with PlanAhead (004088A)

PARTNERS

- This training course is approved by XILINX

PREREQUISITES

- At least six months of design experience with Xilinx tools and FPGAs
- Designing for performance (002833A) course completed
- Xilinx FPGAs architectures knowledge
- Intermediate knowledge of an HDL language

TRAINING MATERIALS

Software Configuration :

- Xilinx ISE Design Suite 13.1 Logic Edition

Recommended Hardware Configuration :

- Intel Core 2 or more recent
- Windows XP or 7
- 1 GB Free disk after software installation
- At least 2Go RAM
- Minimum Display resolution : 1024 x 768
- On Site training : video projector

**XILINX**®Authorized
Training Provider

Contact

Tel : 05 62 13 52 32
Fax : 05 61 06 72 60
training@mvd-fpga.comCourse also available
customized on site

Next sessions, see : <http://www.mvd-training.com/en/schedule.html>

TOPICS

1st day

- Introduction
 - Exercise : Review of timing constraints
- UCF file editing and syntax
 - Exercise
- Advanced IO timing Constraints
 - Exercise
- TCL Script

2nd day

- Exercise
- Floorplanning
 - Exercise
- Design Preservation Techniques
 - Exercise
- FPGA Editor
 - Exercise

DOCUMENTATION

Training manuals will be given to attendees during training in print.