

DSP design with System Generator

Ref : 002836A

Duration : 2 days

OBJECTIVES

- Who should attend ? Engineers and hardware designers who are implementing DSP algorithms using the MathWorks MATLAB® and Simulink® software and want to use Xilinx System Generator for DSP design
- This course allows you to explore the System Generator tool and to gain the expertise you need to develop advanced, low-cost DSP designs
- Describe the System Generator design flow for implementing DSP functions
- Identify Xilinx FPGA capabilities and implement a design from algorithm concept to hardware simulation
- List various low-level and high-level functional blocks available in System Generator
- Identify the high-level blocks available for FIR and FFT designs
- Design a multiple-clock-based System Generator system
- Embed two System Generator designs into a larger design

RELATED COURSES

- DSP implementation techniques for Xilinx FPGAs (002838A)

PARTNERS

- This training course is approved by XILINX

PREREQUISITES

- Experience with MATLAB and Simulink
- Basic understanding of digital signal processing
- Knowledge of Xilinx FPGA DSP resources

TRAINING MATERIALS

Software Configuration :

- Xilinx ISE Design Suite 11.3 DSP Edition
- Matlab with Simulink Software R2008a or R2008b

Recommended Hardware Configuration :

- Intel Core 2 or equivalent
- Windows XP
- 1 GB Free disk after software installation
- At least 1Go RAM
- Minimum Display resolution : 1024 x 768
- On Site training : video projector



Contact

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Course also available
customized

Next sessions, see : <http://www.mvd-training.com/en/schedule.html>

TOPICS

1st Day

- Introduction to System Generator
 - Introduction
 - Design flow
- Simulink Software Basics
 - Stimulus and Response
 - Sample Period
 - Solver
 - Workspace
 - Design Hierarchy and Masked Subsystems
- **Lab 1:** Using the Simulink Software
- Basic Xilinx Design Capture
 - Gateway In and Gateway Out
 - Data types
 - Constructing a design
 - System Generator block
 - HDL Co-Simulation
 - Hardware Verification
- **Lab 2:** Getting Started with Xilinx System Generator
- Signal Routing
 - Signal Conversion
 - Bit picking
 - Reinterpret Block
 - Convert Block
 - Concat Block
 - Slice Block
 - BitBasher Block
 - Expression Block

- **Lab 3:** Signal Routing
- Implementing System Control
 - Control Mechanisms
 - Handling Data Bursts
 - MCode Block
- **Lab 4:** Implementing System Control

2nd Day

- Multi-Rate Systems
 - Sample Rate-Changing blocks
 - Simulink software propagation rules
 - Hardware
- **Lab 5:** Designing a MAC-based FIR
- Filter Design
 - MAC FIR Filters
 - FIR Compiler
 - DA Filters
 - FDATool
- **Lab 6:** Designing a FIR Filter Using the FIR Compiler Block
 - FIR Compiler Block – ML403 Lab
 - DAFIR Block – SP3E Lab
- Xilinx System Generator, Project Navigator, and Platform Studio Integration
 - Introduction
 - Implementing and performing Design Iteration
 - Clocking methodology
 - Creating Base System Builder from XPS and Importing into Sysgen
- **Lab 7:** System Generator and Project Navigator Integration

DOCUMENTATION

Training manuals will be given to attendees during training in print.