

DSP design with System Generator

Ref : 002836A

Duration : 2 days

OBJECTIVES

- Who should attend ? Engineers and hardware designers who are implementing DSP algorithms using the MathWorks MATLAB® and Simulink® software and want to use Xilinx System Generator for DSP design
- Describe the System Generator design flow for implementing DSP functions
- Identify Xilinx FPGA capabilities and how to implement a design from algorithm concept to hardware simulation
- List various low-level and high-level functional blocks available in System Generator
- Use custom boards for hardware co-simulation
- Identify the high-level blocks available for FIR and FFT designs
- Design a multiple-clock-based System Generator system
- Embed two System Generator designs into a larger design

RELATED COURSES

- Essential DSP implementation techniques for Xilinx FPGAs (002838A)

PARTNERS

- This training course is approved by XILINX

PREREQUISITES

- Experience with MATLAB and Simulink
- Basic understanding of digital signal processing
- Knowledge of Xilinx FPGA DSP resources

TRAINING MATERIALS

Software Configuration :

- Xilinx ISE Design Suite 13.1 DSP Edition
- Matlab with Simulink Software R2010b

Recommended Hardware Configuration :

- Intel Core 2 or more recent
- Windows XP or 7
- 1 GB Free disk after software installation
- At least 2Go RAM
- Minimum Display resolution : 1024 x 768
- On Site training : video projector
- ML605 or SP605 board to run hardware co-simulation labs


 Authorized
Training Provider

Contact

 Tel : 05 62 13 52 32
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 Course also available
customized on site

 Next sessions, see : <http://www.mvd-training.com/en/schedule.html>

TOPICS

1st Day

- Introduction to System Generator
 - Introduction
 - Design flow
- Simulink Software Basics
 - Stimulink® and Matlab® Software
 - Stimulus and Response
 - Sample Period and Solvers
 - Workspace
 - Design Hierarchy and Masked Subsystems
 - Lab : Using the Simulink Software
- Basic Xilinx Design Capture
 - Gateway In and Gateway Out
 - Data types
 - Construction a design
 - System Generator block
 - HDL Co-Simulation
 - Hardware Verification
 - Lab : Getting Started with Xilinx System Generator
- Signal Routing
 - Signal Conversion
 - Bit picking
 - BitBasher Block
 - Expression Block
 - Lab : Signal Routing
- Implementing System Control
 - Control Mechanisms

- Handling Data Bursts
- MCode Block
- Lab : Implementing System Control

2nd Day

- Multi-Rate Systems
 - Sample Rate-Changing blocks
 - Simulink software propagation rules
 - Hardware
 - Lab : Designing a MAC-based FIR
- Filter Design
 - MAC FIR Filters
 - FIR Compiler
 - FDATool
 - Lab : Designing a FIR Filter Using the FIR Compiler Block
- Xilinx System Generator, Project Navigator, and Platform Studio Integration
 - Introduction
 - Implementing and performing Design Iteration
 - Clocking methodology
 - Creating Base System Builder from XPS and Importing into Sysgen
 - Lab : System Generator and Project Navigator Integration
- Spartan-6 and Virtex-6 FPGA DSP Platforms
 - DSP Targeted Design Platform (TDP)
 - AXI4 Protocol Overview
 - DSP TDP Reference Design Overview
 - Lab : Application and hardware co-simulation

DOCUMENTATION

Training manuals will be given to attendees during training in print.