

DSP implementation techniques for Xilinx FPGAs

Ref : 002838A

Duration : 3 days

OBJECTIVES

- Who should attend ? Engineers and hardware designers who should develop DSP algorithm using Xilinx FPGA
- Describe how DSP algorithms can be efficiently implemented using Xilinx FPGA technology, particularly using Spartan 3E and Virtex 4
- Evaluate which algorithms are best suited to FPGA implementation and understand which algorithms are less desirable
- Observe how system level decisions impact the hardware implementation, and that the hardware implementation can enhance the results at the system level

RELATED COURSES

- Designing for performance, ISE (002833A)
- DSP Design with System Generator (002836A)
- DSP Design with AccelDSP (004850A)

PARTNERS

- This training course is approved by XILINX

PREREQUISITES

- Fundamental understanding of digital signal processing theory and an appreciation of the principles of the following:
 - Sample rates
 - FIR (Finite Impulse Response) and IIR (Infinite Impulse Response) filters
 - Oscillators and Mixers
 - FFT (Fast Fourier Transform) algorithm

TRAINING MATERIALS

- No computer is necessary. Only a pencil, eraser and calculator are necessary.
- On customer request, some practical exercises using VHDL can be done. But it reduces covered topics. In that case, a good knowledge of ISE and VHDL is strongly recommended.
- On Site training : video projector



Contact

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Course also available
customized

Next sessions, see : <http://www.mvd-training.com/en/schedule.html>

TOPICS

1st day

- Introduction
 - Basic terminology and acronyms used in DSP design
 - Sample rates and bit widths used in DSP applications
 - DSP Building blocks and processing requirements
- Number
 - Numbering formats, range and precision
 - Mathematical operations using a variety of formats
- FPGA Architecture
 - Structure and resources of Xilinx devices
 - Slice structure
 - Arithmetic function implementation
 - Distributed RAM and SRL
 - Estimating DSP building block sizes

2nd day

- FPGA Architecture (continuing)
 - Implementing the multiplication function
 - Slice Implementation
 - Multiplier Blocks and DSP blocks
 - Bit width impact on system level decisions
- Memory

- Block versus Distributed memory
- SRL16E and the delay function
- Memory aspect ratios and their manipulation
- FIR filter specifications
 - FIR filter implementations
 - Parallel implementation
 - Transposed implementation
 - Systolic implementation
 - Selection of a technique for a given specification
 - Effects of halfband and interpolated filters

3rd day

- Specific Filters
 - Options to be considered with multiple channels
 - Interpolation and Decimation
 - Rate changing and how it affects FIR filter choice
 - Filtering algorithms that exploit device architecture
 - Importance of connectivity versus isolated functions
- Others functions commonly used
 - CIC
 - IIR basics
 - Numeric Controlled Oscillators and Mixers
 - Strategies for FFT implementation

DOCUMENTATION

Training manuals will be given to attendees during training in print.