

Essential DSP implementation techniques for Xilinx FPGAs

Ref : 002838A

Duration : 2 days

OBJECTIVES

- Who should attend ? Engineers and hardware designers who should develop DSP algorithm using Xilinx FPGA
- Describe the advantages of using FPGAs over traditional processors for DSP designs
- Utilize fixed point binary arithmetic and identify how to use this knowledge to create efficient designs in FPGAs
- Recognize how both the CLB slices in FPGAs and the more advanced DSP48s are used to implement DSP algorithms
- Explain the dataflow through the device and how to use distributed memory, block RAM, registers, and SRLs to properly implement these designs
- Construct different FIR filter and FFT implementations and how to optimize these implementations in the FPGA
- Explain the algorithms for video and imaging systems and their implementations in FPGAs

RELATED COURSES

- Designing for performance, ISE (002833A)
- DSP Design with System Generator (002836A)
- Spartan 6, ISE (004851A)
- Virtex 6, ISE (004852A)

PARTNERS

- This training course is approved by XILINX

PREREQUISITES

- Fundamental understanding of digital signal processing theory and an appreciation of the principles of the following:
 - Sample rates
 - FIR (Finite Impulse Response) and IIR (Infinite Impulse Response) filters
 - Oscillators and Mixers
 - FFT (Fast Fourier Transform) algorithm

TRAINING MATERIALS

- No computer is necessary. Only a pencil, eraser and calculator are necessary.
- On customer request, some practical exercises using VHDL can be done. But it reduces covered topics. In that case, a good knowledge of ISE and VHDL is strongly recommended.
- On Site training : video projector



Contact

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Course also available
customized on site

Next sessions, see : <http://www.mvd-training.com/en/schedule.html>

TOPICS

1st day

- Back to Basic
 - Traditional DSP vs. FPGA
 - Digital Signal Processing: What, Why, and Where
 - Signed Binary Number Refresher
 - Signed Number Arithmetic
 - Quantization, Saturation, Truncation, and Rounding
 - Latency vs. Throughput
- FPGA Architecture
 - Spartan-6 and Virtex-6 FPGA Overview
 - CLB Architecture
 - DSP48A1/E1
 - Block RAM Memory Resources
- FPGA Math
 - Addition and Subtraction
 - Accumulation
 - Multiplication
 - Other Functions (Virtex-6 FPGA)
 - Lab
- Shift Registers, RAM and Applications
 - SRL32E
 - Distributed Memory
 - Block Memory
 - Lab
- The FIR Filter
 - Overview
 - MAC Engine FIR
 - Semi Parallel FIR
 - Serial Distributed Arithmetic FIR

- Full Parallel FIR
- Parallel Distributed Arithmetic FIR
- FIR Compiler
- Lab

2nd day

- Advanced Filter Techniques
 - Overview
 - Multiple-Channel Filter
 - Halfband and Interpolated Filters
 - Multiple-Rate Filter: Interpolation Theory
 - Multiple-Rate Filter: Decimation Theory
 - Multiple-Channel, Multiple-Rate Filter
 - Other Functions and Filters
 - Lab
- The Fast Fourier Transform
 - Overview
 - FFT Design
 - FFT 7.0 Core
 - Lab
- Video and Imaging
 - Introduction
 - Datapath vs. Post Process
 - Video Processing Techniques
 - Image Processing
- Where do we go from here ?
 - FPGA as a Co-Processor
 - DSP Design Kits
 - DSP Design Tools
 - System Generator Demo
 - CORE Generator Tool Resources

DOCUMENTATION

Training manuals will be given to attendees during training in print.