
Designing with Multi-Gigabit RocketIO Transceivers

Ref : 002843A

Duration : 3 days

OBJECTIVES

- Describe and utilize the ports and attributes of the RocketIO™ multi-gigabit transceiver (GTP, GTX and GTH) in the Virtex™-5/6 and Spartan-6 Family
- Effectively use the following features : 8b/10b and 64b/66b encoding/decoding, channel bonding, clock correction, Comma detection.
- Use the GTP Wizard (Architecture Wizard)
- Synthesis and Implementation considerations
- Usage of ChipScope Serial IO Toolkit and IBERT.

RELATED COURSES

- VHDL Logical Synthesis and Simulation for Xilinx FPGA design (002572A)
- Designing with the Virtex-6 Family (004852A)
- Designing with the Spartan-6 Family (004851A)

PARTNERS

- This training course is approved by XILINX

PREREQUISITES

- Experience of Xilinx FPGA design and simulation
- Intermediate knowledge in VHDL language
- Knowledge of high-speed serial I/O protocols and standards is a plus

TRAINING MATERIALS

Software Configuration :

- Xilinx ISE Design Suite 11.3 Logic Edition

Recommended Hardware Configuration :

- Intel Core 2 or equivalent
- Windows XP
- 1 GB Free disk after software installation
- At least 1Go RAM
- Minimum Display resolution : 1024 x 768
- On Site training : video projector

Authorized
Training Provider

Contact

Tel : 05 62 13 52 32
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training@mvd-fpga.comCourse also available
customized

Next sessions, see : <http://www.mvd-training.com/en/schedule.html>

TOPICS

1st day

- Virtex-6 and Spartan-6 Family Overview
- Transceivers Overview (GTP, GTX, GTH)
- GTP, GTX Clocking and Resets
- 8b/10b encoder and decoder
 - **Lab 1** : 8b/10b Disparity and bypass
- Commas and Deserializer Alignment
 - **Lab 2** : Commas and data alignment

2nd day

- Rx Elastic Buffer and Clock Correction
 - **Lab 3** : Clock Correction
- Channel Bonding

- **Lab 4** : Channel Bonding
- GTP Wizard Overview
- **Lab 5** : GTP Core generation
- Transceiver Implementation and simulation
- **Lab 6** : Implementation and Simulation
- Physical Media Attachments

3rd day

- Virtex-6 GTX 64/66 Encoding and the gearbox
 - **Lab 7** : 64b/66b GTX Transceivers
- Transceiver Board Design
- RocketIO Transceiver test and debugging
 - **Lab 8** : System Lab
- RocketIO Transceiver Application Examples

DOCUMENTATION

Training manuals will be given to attendees during training in print.