

Designing with Multi-Gigabit RocketIO Transceivers

Ref : 002843A

Duration : 3 days

OBJECTIVES

- Describe and utilize the ports and attributes of the RocketIO™ multi-gigabit transceiver in the Spartan™-6 and the Virtex™-6 Family
- Effectively use the following features : 8b/10b and other encoding/decoding, channel bonding, clock correction, comma detection, pre-emphasis and linear equalization.
- Use the transceiver Wizards (Architecture Wizard)
- Synthesis and Implementation considerations
- Usage of ChipScope Serial IO Toolkit and IBERT.

RELATED COURSES

- VHDL Logical Synthesis and Simulation for Xilinx FPGA design (002572A)
- Spartan™-6, ISE (004851A)
- Virtex™-6, ISE (004852A)

PARTNERS

- This training course is approved by XILINX

PREREQUISITES

- Experience of Xilinx FPGA design and simulation
- Intermediate knowledge in VHDL language
- Knowledge of high-speed serial I/O protocols and standards is a plus

TRAINING MATERIALS

Software Configuration :

- Xilinx ISE Design Suite 13.1 Logic Edition

Recommended Hardware Configuration :

- Intel Core 2 or more recent
- Windows XP or 7
- 1 GB Free disk after software installation
- At least 2Go RAM
- Minimum Display resolution : 1024 x 768
- On Site training : video projector

Contact

Tel : 05 62 13 52 32
Fax : 05 61 06 72 60
training@mvd-fpga.com

Course also available
customized on site



Authorized
Training Provider

Next sessions, see : <http://www.mvd-training.com/en/schedule.html>

TOPICS

1st day

- Spartan-6 and Virtex-6 Family
- Transceiver Overview (GTP, GTX, GTH)
- Transceiver Clocking and Resets
- 8b/10b encoder and decoder
 - Lab : 8b/10b Disparity and bypass
- Commas and Deserializer Alignment
 - Lab : Commas and data alignment

2nd day

- Rx Elastic Buffer and Clock Correction
 - Lab : Clock Correction
- Channel Bonding

- Lab : Channel Bonding
- GTP Wizard Overview
 - Lab : GTP Core Generation
- Implementing and simulating a Rocket IO Transceiver Design
 - Lab : Synthesis and Simulation
- Physical Media Attachments

3rd day

- Virtex-6 FPGA GTX 64B/66B Encoding and the Gearbox
 - Lab : 64b/66b GTX Transceivers
- Transceiver board design
- Transceiver test and debugging
 - Lab : System lab / IBERT Lab
- Transceiver Application Examples

DOCUMENTATION

Training manuals will be given to attendees during training in print.