

MPC854X IMPLEMENTATION

Ref : 002881A

Duration : 5 days

OBJECTIVES

- The course focuses on the Ocean crossbar that interconnects e500, RapidIO, DDR SDRAM, PCI and external bus
- Cache coherency protocol is introduced in increasing depth
- The 64-bit e500 core is viewed in detail, especially the SPU that enables Floating point and vector processing
- The boot sequence and the clocking are explained
- The course focuses on hardware implementation of the MPC8540
- A long introduction to DDR SDRAM operation is done before studying the DDR SDRAM controller
- An in-depth description of the RapidIO port and the PCI-X port is performed
- The course highlights both hardware and software implementation of gigabit / fast / Ethernet controllers

RELATED COURSES

- RapidIO bus (002602A)
- PCI bus (002596A)

PARTNERS

- This training course is approved by FREESCALE

PREREQUISITES

- Experience of a 32 bit processor or DSP is recommended
- Knowledge of the RapidIO and PCI bus is recommended

**WIND RIVER****NeoMore**

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Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

INTRODUCTION TO THE MPC8540

- Internal data flows, OCEAN switch fabric, packet reordering
- Address map, ATMU
- Local vs external address spaces, inbound and outbound address decoding
- System performance monitor

THE e500 CORE

- Differences between the new Book E architecture and the classic PowerPC architecture
- The instruction pipeline
- Dynamic branch prediction
- The first level MMU and the second level MMU
- The L1 caches
- Cache coherency : MEI vs MESI state machine
- Level 2 cache, partition into 128-kb L2 cache plus 128-kb SRAM
- The Core Complex Bus
- Load store unit, data buffering between LSU and CCB
- Signal Processing APU (SPU)
- PowerPC EABI : sections, C-to-assembly interface
- Book E exception handling
- Core timers : Dec, TB, FIT and Software Watchdog
- Power management
- Performance monitoring, counting of events
- JTAG emulation, real time trace when the e500 core executes cached instructions

RESET, CLOCKING AND INITIALIZATION

- Platform clock
- RapidIO transmit clock source selection
- Power-on reset sequence, use of the I2C interface to access serial ROM
- Power management

THE DDR-SDRAM CONTROLLER

- DDR-SDRAM operation : a 128-Mbits DDR-SDRAM from Micron is used as an example
- Command truth table
- Bank activation, read, write and precharge timing diagrams, page mode
- ECC error correction
- DDR-SDRAM controller introduction
- Initial configuration following Power-on-Reset
- Initialization routine

DOCUMENTATION

- Training manuals will be given to attendees during training in print.

LOCAL BUS CONTROLLER

- Multiplexed 32-bit address and data transfers
- Burst support
- Dynamic bus sizing
- GPCM, UPMs and SDR SDRAM states machines

RapidIO INTERFACE UNIT

- 8-pin parallel interface, LVDS signalling
- Reordering across priority levels
- Packet pacing support at the physical layer
- RapidIO compliant message unit

PCI/PCI-X FUNCTIONAL UNITS

- Data flows : Read prefetch and write posting FIFOs
- Inbound transactions handling, Outbound transactions handling in both modes
- Support of multiple split transactions in PCI-X mode
- PCI-to-memory and memory-to-PCI streaming

LOW SPEED PERIPHERALS

- Programmable Interrupt Controller
- Description of the 4 timers / counters
- Message interrupts
- Description of the NS16450/16550 compliant Uarts
- I2C protocol fundamentals
- Transmission and reception sequence

THE ETHERNET CONTROLLERS

- 802.3 specification fundamentals : the 3 layers PHY, MAC and control
- The ENET controllers
- Address recognition, pattern matching
- MII interface
- the three-speed Ethernet controllers (TSECs)
- Physical interfaces : GMII, MII, TBI or RGMII
- Buffer descriptor management
- Layer 2 acceleration

INTEGRATED DMA CONTROLLER

- Scatter / gathering
- Ability to start DMA from external 3-pin interface