

## MPC8560 SOFTWARE IMPLEMENTATION

Ref : 002882A

Duration : 5 days

### OBJECTIVES

- The course focuses on the Ocean crossbar that interconnects e500, RapidIO, DDR SDRAM, PCI and external bus
- Cache coherency protocol is introduced in increasing depth
- The 64-bit e500 core is viewed in detail, especially the SPU that enables Floating point and vector processing
- The boot sequence and the clocking are explained
- The course highlights both hardware and software implementation of gigabit / fast / Ethernet controllers
- The course describes the Time Slot Assigner initialization in order to handle E1 frames
- The MCC superchanneling is examined

### RELATED COURSES

- The training 002602A covers the RapidIO bus
- The training 002596A covers the PCI bus and the training 002597A handles the PCI-X extension
- The training 002883A handles the hardware implementation of the MPC8560

### PREREQUISITES

- Experience of a 32 bit processor or DSP is recommended
- Knowledge of the RapidIO and PCI bus is recommended

### PARTNERS

- This training course is approved by FREESCALE


**WIND RIVER**

**NeoMore**

### Contact

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Course also available  
 customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

### TOPICS

#### INTRODUCTION TO THE MPC8560

- Internal data flows, OCEAN switch fabric, packet reordering
- Address map, ATMU
- Local vs external address spaces, inbound and outbound address decoding
- Accessing CCSR memory from external master

#### THE e500 CORE

- The instruction pipeline
- Dynamic branch prediction
- The first level MMU and the second level MMU
- Process protection
- The L1 caches
- Level 2 cache
- e500 coherency module
- Load store unit, data buffering between LSU and CCB
- Signal Processing APU (SPU)
- PowerPC EABI
- Book E exception handling
- Power management
- JTAG emulation

#### RESET, CLOCKING AND INITIALIZATION

- Platform clock
- Power-on reset sequence, use of the I2C interface to access serial ROM
- Boot page translation

#### BASICS OF HARDWARE IMPLEMENTATION

- DDR-SDRAM controller
- Local bus controller
- RapidIO interface unit
- PCI/PCI-X functional unit
- Software implementation of these units

#### LOW SPEED PERIPHERALS

- Programmable Interrupt Controller
- Interrupt nesting
- Description of the 4 timers / counters
- Message interrupts
- I2C controller

### DOCUMENTATION

- Training manuals will be given to attendees during training in print.

#### THE THREE-SPEED ETHERNET CONTROLLERS TSECs

- Physical interfaces : GMII, MII, TBI or RGMII
- Buffer descriptor management
- Layer 2 acceleration accept or reject on address or pattern match
- 256-entry hash table for unicast and multicast
- Direct queuing of four flows

#### INTEGRATED DMA CONTROLLER

- Priority between the 4 channels
- Scatter / gathering
- Selectable hardware enforced coherency

#### CPM INTRODUCTION

- CP operation : peripheral prioritization
- Command register
- DPRAM organization
- IDMA vs SDMA

#### THE SERIAL INTERFACE

- NMSI versus TDM
- MCC connection to SI
- Baud rate generators
- Communication initialization sequence
- Buffer descriptor ring allocation in DPRAM
- Buffer chaining

#### THE MULTI CHANNEL CONTROLLERS

- DPRAM organization
- Time slot vs logic channel
- Super channels
- HDLC channel parameters
- Interrupt queues

#### THE SERIAL COMMUNICATION CONTROLLERS

- Data encoding /decoding selection
- Hardware flow management
- HDLC on SCC
- Ethernet on SCC : address recognition, hash table programming

#### FAST ETHERNET CONTROLLER

- 802.3u basics
- MII interface
- Hash tables utility
- Parameter RAM description