

MPC 8560 HARDWARE IMPLEMENTATION

Ref : 002883A

Duration : 2 days

OBJECTIVES

- The course focuses on the Ocean crossbar that interconnects e500, RapidIO, DDR SDRAM, PCI and external bus
- Cache coherency protocol is introduced in increasing depth
- The boot sequence and the clocking are explained
- The course focuses on hardware implementation of the MPC8560
- A long introduction to DDR SDRAM operation is done before studying the DDR SDRAM controller
- An in-depth description of the RapidIO port and the PCI-X port is performed
- The course highlights both hardware and software implementation of gigabit / fast / Ethernet controllers

RELATED COURSES

- RapidIO bus (002602A)
- PCI bus (002596A)
- MPC8560 software implementation 002882A

PREREQUISITES

- Experience of a 32 bit processor or DSP is recommended
- Knowledge of the RapidIO and PCI bus is recommended

PARTNERS

- This training course is approved by FREESCALE

**WIND RIVER****NeoMore**

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Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

INTRODUCTION TO THE MPC8560

- Implementation examples
- Internal data flows, OCEAN switch fabric, packet reordering
- Address map, ATMU
- Local vs external address spaces, inbound and outbound address decoding
- Accessing CCSR memory from external master

MAIN FEATURES OF THE e500 CORE

- The L1 caches, PLRU replacement algorithm, 8-way set associativity
- Cache coherency : MEI vs MESI state machine
- Level 2 cache, partition into 128-kb L2 cache plus 128-kb SRAM
- Allocation of data transferred by external masters into the cache
- e500 coherency module
- The Core Complex Bus : high speed on-chip local bus with data tagging
- Exception handling
- JTAG emulation, real time trace when the e500 core executes cached instructions

RESET, CLOCKING AND INITIALIZATION

- Platform clock
- RapidIO transmit clock source selection
- Power-on reset sequence, use of the I2C interface to access serial ROM
- Power-on reset configuration
- Boot page translation

THE DDR-SDRAM CONTROLLER

- DDR-SDRAM operation : a 128-Mbits DDR-SDRAM from Micron is used as an example
- Jedec specification basics, mode register initialization, bank selection and precharge

DOCUMENTATION

- Training manuals will be given to attendees during training in print.

- Command truth table
- Bank activation, read, write and precharge timing diagrams, page mode
- DDR-SDRAM controller introduction
- Initial configuration following Power-on-Reset
- Address decode
- Timing parameters programming
- Initialization routine

LOCAL BUS CONTROLLER

- Multiplexed 32-bit address and data transfers
- Burst support
- Dynamic bus sizing
- GPCM, UPMs and SDR SDRAM states machines

RapidIO INTERFACE UNIT

- 8-pin parallel interface, LVDS signalling
- Packet pacing support at the physical layer
- Atomic operations
- RapidIO compliant message unit

PCI/PCI-X FUNCTIONAL UNITS

- Data flows : Read prefetch and write posting FIFOs
- Inbound transactions handling, outbound transactions handling in both modes
- Support of multiple split transactions in PCI-X mode
- PCI-to-memory and memory-to-PCI streaming

HARDWARE IMPLEMENTATION OF COMMUNICATION

- Ethernet physical interfaces : GMII, MII, TBI or RGMII
- Configuration of the TDM lines interface
- Description of the Utopia interface