

## MPC 824X IMPLEMENTATION

Ref : 002885A

Duration : 5 days

### OBJECTIVES

- The course describes various implementation of the MPC824X : PCI host and PCI IO device
- The course details the address translation mechanism used to access from core to PCI and from PCI to SDRAM
- The course focuses on assembly programming and EABI understanding
- The hardware implementation is studied, particularly the SDRAM controller
- The course explains the scatter / gather operation of the DMA channel
- Synchronization between masters through message is highlighted

### RELATED COURSES

- PCI bus (002596A)

### PARTNERS

- This training course is approved by FREESCALE

### PREREQUISITES

- Experience of a 32 bit processor or DSP is recommended



### Contact

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Course also available  
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

### TOPICS

#### INTRODUCTION TO THE MPC824X

- internal data paths, CCU operation
- benefits of the snoopers, sharing of cache enabled regions
- Differences between MPC8240 and MPC8245

#### ADDRESS TRANSLATION

- Address translation from core to PCI Memory space
- Address translation from PCI to SDRAM
- Selection of the base address of internal memory mapped status and control registers

#### RESET SEQUENCE

- Self configuration of the MPC824X through input sampling
- Requirements of the boot routine

#### THE PPC603e CORE

- 603e pipeline introduction
- instruction queue, superscalar execution, register renaming, out-of-order execution
- Dispatch conditions, completion conditions
- FPU and LSU internal pipeline operation
- Execution serialization
- Branch management : static prediction
- Guarded memory

#### L1 CACHES

- Cache basics
- Cache related page / block attributes
- 603e L1 cache : LRU algorithm, H1D0 programming interface
- Software L1 data cache flush
- Cache coherency : the MEI 3-bit L1 data line state
- MEI snooping sequences involving the 603e core and a PCI master

#### THE UISA LAYER

- Branch instructions
- Integer load / store instructions, boolean semaphore management
- Integer arithmetic and logic instructions
- IEEE754 basics
- FPU operation
- The EABI
- Code and data sections, small data areas benefits

#### THE VEA LAYER

- Cache related instructions
- PowerPC timers : TB and DEC

### DOCUMENTATION

- Training manuals will be given to attendees during training in print.

#### THE OEA LAYER - MMU

- MMU goals
- The PowerPC address processing : real mode, bloc address translation, segment / page mode
- WIMG attributes definition
- Process protection through VSID selection
- TLB organization
- Page translation
- MMU implementation in real-time sensitive applications

#### THE OEA LAYER - EXCEPTION MECHANISM

- Exception state saving and restoring
- Exception management
- Recoverable vs non recoverable interrupts
- Requirements to support exception nesting

#### INTEGRATED DEBUG FACILITIES

- Tagging of the master accessing SDRAM
- Hardware vs software breakpoint
- JTAG emulation
- Real time trace requirements

#### HARDWARE IMPLEMENTATION

- Pinout
- Clocking, selection of the PLL ratio
- DLL benefit, electrical interface

#### THE MEMORY CONTROLLER

- SDRAM basics, page mode, refresh, timing diagrams
- SDRAM related registers initialisation according to IBM SDRAM device features
- The Flash EPROM controller
- Port-X

#### THE PCI INTERFACE

- Commands supported when the MPC824X is a PCI master and when the MPC824X is a PCI target
- Access to the local SDRAM address space by a PCI master
- Generation of configuration transactions

#### INTERNAL PERIPHERALS

- The interrupt controller
- Internal timers
- Synchronization mechanisms : doorbell registers, I2O compliant messaging
- The DMA controller, selection of the command generated on the PCI side
- The I2C controller