

MCF 5282 IMPLEMENTATION

Ref : 002888A

Duration : 3 days

OBJECTIVES

- Optimized code writing based on pipeline knowledge
- Memory controller understanding, especially SDRAM controller
- Implementation of a UART to Ethernet communication link
- Boot from flash
- Programming of a sequence of analog to digital conversions

RELATED COURSES

- The course 002601A explains the operation of the **CAN bus**
- For programmers having to develop a BSP or a driver, the course 002603A called **C language for real time and embedded applications** is recommended

PREREQUISITES

- Experience of a 32 bit processor or DSP is mandatory

PARTNERS

- This training course is approved by FREESCALE



Contact

Tel : 05 62 13 52 32
Fax : 05 61 06 72 60
training@mvd-fpga.com

Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

THE V2 COLD FIRE CORE

- ColdFire core versions
- V2 pipeline
- Description of assembly instructions
- Mac instructions, implementation of a fixed point DFT
- ColdFire instruction set architecture enhancements
- Stack management, subroutine call and return
- C to assembly interface, organization of the stack frame
- Section definition
- Exception management
- 5282 2-kb cache operation, direct-mapped organization
- Cache coherency and invalidation, software control
- Internal 64-kb SRAM
- 512-kb Flash module map, program, erase and verify sequences, CFM configuration field, security key
- Power management

DEBUG FACILITIES

- Intrusive vs non-intrusive debug
- BDM port
- Hardware breakpoints
- Trace port

RESET

- Reset control flow
- Chip mode selection
- Boot device selection
- Configuration of the General Purpose Input / Output pins

DEVICE CONFIGURATION

- System Control Module, software watchdog, selection of Internal Peripheral System Base Address
- Internal bus arbitration
- Clocking
- The interrupt controllers

HARDWARE IMPLEMENTATION

- Dynamic bus sizing
- Address decoding
- External master interface
- Bus error management
- The memory controller

- The SDRAM controller

TIMERS

- Programmable Interrupt Timer Modules
- General Purpose Timer Modules
- DMA timers

THE DMA CONTROLLER

- Dual address transfers, continuous-mode or cycle-steal transfers
- Auto-alignment
- Hardware initiated transfers
- Burst transfers
- Automatic transfer of characters received or transmitted by an UART through a DMA channel

COMMUNICATION CONTROLLERS

The 3 UARTs

- Connection with DMA channels
- Transmit and receive sequences

The QSPI

- SPI protocol basics
- Command queue
- Transmit and receive sequences

The I2C controller

- I2C protocol basics
- Transmit and receive sequences

The FlexCAN controller

- CAN protocol basics
- Message buffers
- Mask registers
- Receive and Transmit processes

The Fast Ethernet Controller

- Ethernet basics
- MII hardware interface
- Buffer management, buffer chaining
- Address filtering, use of hash tables
- Full duplex operation, flow control
- Receive and transmit sequences

QADC MODULE

- Conversion queue priority scheme
- Hardware interface
- External trigger

- Result formats
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DOCUMENTATION

Training manuals will be given to attendees during training **both in pdf and in print**. Precise and easy to use, those notes can be used as a reference afterwards.

CONTACT INFORMATIONS

Web site : <http://www.mvd-fpga.com>

E-mail : training@mvd-fpga.com

Tel : +33 (0) 5 62 13 52 32

Fax : +33 (0) 5 61 06 72 60