Virtex PowerPC System Implementation

Ref : 002952A **Duration : 4 days**

OBJECTIVES

- Who should attend ? Engineers and designers who need to develop SoC based on PowerPC and Xilinx FPGA using EDK (Embedded Development Kit)
- Xilinx FPGA provides a new level of system design. This training give necessary knowledge to quickly develop an embedded system using EDK. PPC440 functionalities are also explained
- Develop a project to understand the hardware and the software flow
- Optimization using customer IP is covered
- Software and hardware debug are used. Co-debug is also demonstrated

RELATED COURSES

- C language for real-time and embedded applications (002603A).
- VHDL Logical Synthesis and Simulation for Xilinx FPGA (002572A)
- Microblaze system implementation (003149A)

PARTNERS

- This training course is approved by XILINX

PREREQUISITES

- Experience of a 32 bit processor or DSP is recommended
  - Processor Architecture
  - C language for embedded applications
- Experience of FPGA design using VHDL is recommended
- Experience of system architecture is a plus

TRAINING MATERIALS

Software Configuration :

- Xilinx ISE Design Suite 11.3 Embedded Edition

Recommended Hardware Configuration :

- Intel Core 2 or equivalent
- Windows XP
- 1 GB Free disk after software installation
- At least 1Go RAM
- Minimum Display resolution : 1024 x 768
- On Site training : video projector

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Course also available customized

Next sessions, see : *http://www.mvd-training.com/en/schedule.html*

TOPICS

1st day

- Various System On Chip offered By Xilinx
  - Picoblaze
  - Microblaze
  - PowerPC
- The PPC440 CORE Architecture
  - Pipeline
  - MMU
  - Cache
  - Synchronization
- Hardware Implementation of the PPC440 Core
  - Clock and Power Management
  - Interrupt controller
  - DCR Interface
  - CrossBar
  - PLB interface
  - Memory Controller Interface
  - DMA/LocalLink interface
  - JTAG interface
  - Debug and Trace interface
  - Internal Timer

2nd day

- EDK
  - Introduction
  - XPS
  - SDK
- The Hardware Flow
  - .MHS file
  - SoC hardware platform Specification
  - Peripheral definition files
  - Plagen and implementation tools
- Lab 1 : Hardware Description of a SoC

3rd day

- PowerPC EABI
  - Registers file
  - EABI
  - Sections and C-Start
  - Linker Script
- The Software Flow
  - Executable generation steps
  - .MSS file
  - SoC Software platform Specification
  - Xilinx Peripheral drivers
  - CSP
  - Xilinx Libraries
  - Libgen
  - Application Software
  - Memory initialization
- Lab 2 : Software Description of a SoC

4th day

- Integrated Debug Facilities
  - Introduction
  - Debug registers
- Debugging a PowerPC Application
  - SDK
  - XMD
  - Chipscope Pro
- Optimization
  - IPIF services
  - Create/Import peripheral wizard
- Demo : Debug/IP Creation

DOCUMENTATION

Training manuals will be given to attendees during training in print.