

Microblaze System Implementation

Ref : 003149A

Duration : 4 days

OBJECTIVES

- Who should attend ? Engineers and designers who need to develop SoC based on Microblaze and Xilinx FPGA using EDK (Embedded Development Kit)
- Xilinx FPGA provides a new level of system design. This training give necessary knowledge to quickly develop an embedded system using EDK. Microblaze functionalities are also explained
- Develop a project to understand the hardware and the software flow
- Optimization using customer IP is covered
- Software and hardware debug are used.
- Practical labs will be compiled using GNU tools and downloaded on the Virtex-5 FXT ML507 demo board using the Xilinx Probe

RELATED COURSES

- C language for real-time and embedded applications (002603A).
- VHDL Logical Synthesis and Simulation for Xilinx FPGA (002572A)
- Virtex PowerPC system implementation (002952A)

PARTNERS

- This training course is approved by XILINX

PREREQUISITES

- Experience of a 32 bit processor or DSP is recommended
 - Processor Architecture
 - C language for embedded applications
- Experience of FPGA design using VHDL is recommended
- Experience of system architecture is a plus

TRAINING MATERIALS

Software Configuration :

- Xilinx ISE Design Suite 11.3 Embedded Edition

Recommended Hardware Configuration :

- Intel Core 2 or equivalent
- Windows XP
- 1 GB Free disk after software installation
- At least 1Go RAM
- Minimum Display resolution : 1024 x 768
- On Site training : video projector

Authorized
Training Provider

Contact

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Course also available
customized

Next sessions, see : <http://www.mvd-training.com/en/schedule.html>

TOPICS

1st day

- Various System On Chip offered By Xilinx
 - Picoblaze
 - Microblaze
 - PPC405/PPC440
- The Microblaze Core Architecture
 - Pipeline
 - Load/Store architecture
 - Harvard Architecture
 - Cache Unit
 - MMU
 - Registers file
 - Exceptions mechanism
 - FSL Interface
 - Floating Point Unit
 - Instruction Set Resume
- Microblaze Connections and Parameters
 - LMB Bus
 - PLB Bus
 - FSL Bus
 - XCL Bus
 - Others IO
 - Core configuration

2nd day

- EDK
 - Introduction
 - XPS
 - SDK
- The Hardware Flow
 - .MHS file
 - SoC hardware platform Specification

- Peripheral definition files
- Plagen
- Lab 1 : Hardware Description of a SoC

3rd day

- EABI
 - Introduction
 - Data types
 - Registers usage convention
 - Stack frame
 - Sections
 - Linker script file
- The Software Flow
 - Executable generation steps
 - .MSS file
 - SoC Software platform Specification (SDK)
 - Xilinx Peripheral drivers
 - CSP
 - Xilinx Libraries
 - Libgen
 - Application Software (SDK)
 - Memory initialization
- Lab 2 : Software Description of a SoC

4th day

- Debugging a Microblaze Application
 - Debugging with SDK
 - XMD advanced functionalities
 - Chipscope Pro
- Optimization
 - Introduction
 - Create/Import peripheral wizard
- Demo : Debug/IP Creation

DOCUMENTATION

Training manuals will be given to attendees during training in print.