

## PPC970FX implementation

Ref : 003150A

Duration : 5 days

### OBJECTIVES

- The course details the pipeline operation in order to determine code optimisation guidelines
- Data flows between SDRAM, L1 caches and L2 cache are highlighted
- MERSI cache coherency protocol is introduced in increasing depth
- The operation of the elastic bus is described
- Through a FFT algorithm, the instructor shows how to vectorize processing and reduce execution time using data streaming
- The performance monitor is used to optimise the performance of the FFT

### RELATED COURSES

- The HyperTransport bus training (reference 003153A) may be recommended since most PPC970FX boards are based on this bus

### PREREQUISITES

- Attendees are assumed to be familiar with 32-bit PowerPC architecture

### PARTNERS

- This training course is approved by IBM microelectronics

### Contact

Tel : 05 62 13 52 32  
Fax : 05 61 06 72 60  
training@mvd-fpga.com

Course also available  
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

### TOPICS

#### OVERVIEW

- Functional units
- Key features

#### PPC970 PIPELINE

- Pipeline basics
- Deeply pipelined design, superscalar implementation, register renaming
- Branch prediction mechanism
- Instruction decode and preprocessing
- Instruction dispatch, sequencing and completion control, register renaming
- Dispatch group organization
- Synchronization-based instruction grouping
- Instruction latencies and throughputs
- Software optimisation guidelines

#### MEMORY MANAGEMENT UNIT

- MMU goals
- Data address translation, 128-entry Data ERAT, ERAT Miss Queue
- Second-level Memory Management Unit consisting of SLB and TLB
- 1024-entry 4-way set associative TLB, 64-entry fully associative SLB
- Large page support
- Real memory limit register
- Hypervisor vs supervisor
- Support for 32-bit operating systems

#### INTERNAL DATA FLOWS

- Data paths between load / store units, instruction queue, L2 and external bus
- Out-of-order and speculative issue of load operations
- 32-entry real address based store queues
- 32-entry load re-order queue, tracking of the order of loads
- 8-entry load miss queue
- GUS subsystem
- Core Interface Unit
- L2 cache controller,
- Non Cacheable Unit
- Storage access ordering

- Hardware controlled data prefetch
- Prefetch startup sequence, stream detection
- Synchronization instructions sync, lwsync, ptesync

#### L1 AND L2 CACHES

- Cache basics
- 64 kB direct-mapped instruction cache
- 32 kB 2-way set associative data cache, FIFO replacement policy, Store-through policy
- 512 kB L2 cache, fully inclusive of L1 data caches, MERSI coherency protocol
- Cache coherency, MERSI cache line state, cache state transition tables

#### PROGRAMMING

- Branch instructions
- The system call communication path between applications and RTOS
- Integer load / store instructions
- Integer arithmetic and logic instructions
- IEEE754 basics
- FPU operation : FPSCR register
- Float load / store instructions, floating point exceptions
- Float arithmetic instructions
- The EABI
- Code and data sections, small data areas benefits
- 970FX specific registers

#### THE PERFORMANCE MONITOR

- Objectives
- Event selection
- Configuring the performance monitor bus
- Instruction matching and sampling, the 3 stages of eligibility

#### EXCEPTION MECHANISM

- Exception recognition and priorities
- Focus on soft patch and maintenance exceptions
- Registers updating according to the exception cause
- Requirements to support exception nesting
- Precise processing of machine check exceptions

#### VMX IMPLEMENTATION

- VMX introduction, SIMD processing

- Intra vs inter element instructions
- VMX registers, VSCR initialization
- ANSI C extension to support vector operators, new C types, new castings, vector declaration and initialization
- VMX implementation on the PPC970FX
- Data streams management
- EABI extension to support VMX

**POWER AND THERMAL MANAGEMENT**

- Clocking, PLL design
- Time Base and decremter

- Frequency and voltage scaling
- Additional dynamic power management

**HARDWARE IMPLEMENTATION**

- Unidirectional point-to-point bus segments, source synchronized transfers
  - Packet protocols
  - Snoop response
  - Pipelined transactions
  - Power-on procedure
  - Electrical interface
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**DOCUMENTATION**

Training manuals will be given to attendees during training **both in pdf and in print**. Precise and easy to use, those notes can be used as a reference afterwards.

**CONTACT INFORMATIONS**

**Web site** : <http://www.mvd-fpga.com>

**E-mail** : [training@mvd-fpga.com](mailto:training@mvd-fpga.com)

**Tel** : +33 (0) 5 62 13 52 32

**Fax** : +33 (0) 5 61 06 72 60