

eTPU PROGRAMMING

Ref : 003199A

Duration : 3 days

OBJECTIVES

- The course explains the CPU like TPU architecture
- CPU-TPU interface description
- The course highlights all channel operation modes
- The course focuses on various fields of the instructions enabling concurrency
- The scheduler priority algorithm is detailed in order to estimate the worst case latency for channel service
- Micro-coding and debugging an application composed of several states

RELATED COURSES

- Freescale MCU integrating an eTPU details
 - MPC5xx course 002591A
 - MPC5xx course 003151A
 - ColdFire MCF523x course 003440A

PARTNERS

- This training course is approved by FREESCALE
- Labs are done with Ash Ware tools

PREREQUISITES

- Basic knowledge about microprocessor architecture, hardware timer and assembler instructions and directives



Contact

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Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

INTRODUCTION TO TPU

- Locating the TPU in different components proposed by Freescale
- Objectives of a such approach
- Quick presentation of standard functions

TPU ARCHITECTURE

- The various modules and interactions between them
- Micro-engine
- Ram
- Host interface
- Rom
- Channel
- Scheduler

CHANNEL DESCRIPTION

- Features
- Block diagram
- State at Reset
- Configuring a channel
- Transition event
- Match event
- Full default modes study
- Filter
- Channel link

RAM PARAMETER

- Mapping
- The addressing modes
- Timing
- Coherency

SCHEDULER ARCHITECTURE

- Sources of service requests
- Requests hierarchy
- Preemptivity
- State selection

TPU MICROCODE OVERVIEW

- VLIW machine
- Instruction format

MICRO-ENGINE PROGRAMMING MODEL

- Registers list
- Execution unit hardware
- Code condition latch
- Channel selection
- Loop
- Arithmetic instructions
- Multiply and Mac instructions

FLOW CONTROL INSTRUCTIONS

- Pipeline
- Branch chart
- Conditional branches
- Flush pipe or not
- Repeat capabilities
- Call and return instructions

THE ENTRY POINTS

- Entry table chart
- Scheduler behavior, inner channel priority management
- Entry directive
- Entry points general format

THE SCHEDULER OPERATION

- Sources of service request
- Service requests priority
- Selected state address generation
- Priority scheme

CHANNEL SERVICE WORST CASE LATENCY

- Threads switch timing
- Taking into consideration other requests
- Access concurrency delay

TOOLS PRESENTATION

- ASHWARE eTPU Compiler
- LAUTERBACH debug probe
- Integrated debug facilities

DEFINE AND DEBUG AN APPLICATION

- This part may be tailored to customers needs during on-site training

DOCUMENTATION

- Training manuals will be given to attendees during training in print.