

PPC750Cxe/FX/GX implementation

Ref : 003278A

Duration : 5 days

OBJECTIVES

- The training aims to understand the PowerPC programming environment through the 750 processor
- A focus is done on the PowerPC EABI which is fundamental when C programs are to be interfaced with assembly routines
- The pipeline is viewed in detail in order to infer instructions scheduling guidelines
- Many Diab Data PowerPC specific compiler options are studied
- A flush routine is used to explain data flows between L1 data cache, L2 cache and SDRAM main memory
- The course details the segmentation / pagination mechanism used to protect process
- A generic exception handler is described
- The hardware implementation is also covered
- The course emphasizes differences between 750Cxe, 750FX and 750GX

RELATED COURSES

- The training called "C language for real-time and embedded applications" is recommended for persons in charge of low level software development. Its reference is 002603A

PREREQUISITES

- Experience of a 32 bit processor or DSP is mandatory

PARTNERS

- This training course is approved by IBM microelectronics

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Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

THE INSTRUCTION PIPELINE

- 750 implementation : superscalar operation, out-of-order execution, register renaming, serializations, isync instruction
- Branch processing unit : BTIC, guarded memory
- Branch instructions
- Coding guidelines

DATA PATHS

- Load / store architecture
- Data path between L1 and L2
- Load / store buffers
- Sync and eieio instructions
- Store gathering mechanism

CACHES

- Cache basics
- L1 caches : PLRU algorithm
- Miss under miss operation
- Shared resource management
- Cache coherency mechanism, snooping, related signals
- The MEI state machine
- Management of cache enabled pages shared with PCI DMAs
- Reservation coherency
- Cache related instructions
- Cache flush routine
- The L2 cache, organization, replacement algorithm
- L2 cache locking by way (750FX, 750GX)

SOFTWARE IMPLEMENTATION

- PowerPC architecture specification, the 3 books UISA, VEA and OEA
- addressing modes
- Integer instructions
- IEEE754 basics, floating points numbers encoding
- Floating point arithmetical instructions
- Improvements implemented in the 750FX : additional reservation station and quicker reciprocal estimates
- The PowerPC EABI
- Linking an application with Diab Data

THE MMU

- Thread vs process
- Introduction to real, block and segmentation / pagination translations
- Memory attributes and access rights definition
- Virtual space benefit, page protection through segmentation
- TLBs organization
- Segmentation : process ID definition
- Pagination : PTE table organization
- Explanation of hash value and API field
- MMU implementation in real-time sensitive applications

THE EXCEPTION MECHANISM

- Save / restore registers SRR0/SRR1, rfi instruction
- Exception management mechanism
- Requirements to allow exception nesting
- PowerPC timers TB and DEC

HARDWARE IMPLEMENTATION

- Hreset vs Sreset
- Clocking
- Bus operation
- Address phase
- Data phase
- Address decode logic design
- Timing analysis
- Minimal implementation
- Low power modes
- Power, dual PLLs for seamless frequency switching (750FX, 750GX)

THE PERFORMANCE MONITOR

- Objectives of the performance monitor
- Event counting
- Programming interface

THE DEBUG PORT

- JTAG emulation
- Real time trace requirements

- Code instrumentation
 - Hardware breakpoints
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DOCUMENTATION

Training manuals will be given to attendees during training **both in pdf and in print**. Precise and easy to use, those notes can be used as a reference afterwards.

CONTACT INFORMATIONS

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