

## PCI EXPRESS GEN1, GEN2 et GEN3

Ref : 003279A

Duration : 3 days

### OBJECTIVES

- Packet switching benefits compared to shared busses are highlighted
- The course explains the various traffic types that PCI Express supports
- The use of virtual channels to match Quality of Service requirements is explained
- The course describes the discovery sequence required to initialize the switches
- The course details the various stages of the physical layer : 8b10b and 12B/130b coding, scrambling, elastic buffer, clock recovery and link training sequence
- The course highlight the differences between the 3 generations of PCI Express

### PREREQUISITES

- Experience of a high speed digital bus like PCI / PCI-X is strongly recommended

### RELATED COURSES

- PCI 3.0 bus (004853A)

 **XILINX** | Authorized Training Provider

### Contact

Tel : 05 62 13 52 32  
Fax : 05 61 06 72 60  
training@mvd-fpga.com

Course also available  
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

### TOPICS

#### THE TRANSITION TO PACKET SWITCHING

- PCI bus limitations
- The hub link bus
- Solutions to increase the performance : differential transmission, packet switching

#### INTRODUCTION TO PCI EXPRESS

- Overview
- Topology
- Layer protocol
- Quality of Service
- The physical layer

#### THE PHYSICAL LAYER

- 8-bit / 10-bit coding
- Scrambling
- The ordered sets
- Elastic buffer operation
- Link training, detailed step-by-step sequence
- Jitter budgeting and measurement
- The electrical interface
- Calibration channel characteristics

#### POWER MANAGEMENT

- Link state power management
- PCI Power Management software interface
- Native PCI Express power management mechanisms
- Power budgeting capability

#### PACKET ROUTING

- PCI basics
- Operation of PCI-to-PCI transparent bridge
- Packet routing by the address
- Packet routing by the ID
- Packet routed implicitly

#### TLP ACKNOWLEDGEMENT

- Acknowledgement objectives
- Counters / timers present in the transmitter and the receiver
- Sequences
- Cut-through switches

#### QUALITY OF SERVICE

- Introduction, traffic differentiation

- VC arbitration
- Port arbitration, switch model

#### FLOW CONTROL

- Overview, transmit credit principle
- Related counters
- Credit update frequency

#### TRANSACTION ORDERING

- PCI Producer / Consumer model
- Relaxed ordering permitted by PCI-X
- PCI Express transaction ordering rules

#### PACKET FORMAT

- Benefits of a packet oriented protocol
- TLP format
- DLLP format

#### INTERRUPT MANAGEMENT

- Message Signaled Interrupts
- PCI Express Interrupt Management

#### ERROR MANAGEMENT

- General principles
- PCI-like error management
- PCI Express basic error management
- PCI Express basic advanced error management

#### THE CONFIGURATION SPACE

- Root Complex Register Block [RCRB]
- PCI Express enumeration
- PCI-compatible configuration registers
- Expansion ROMs

#### DIFFERENCES BETWEEN GEN1, GEN2 and GEN3

- The new physical layer of GEN2 and GEN3 with a 12B/130b encoding
- The new protocol transactions
- The new PCI Express Enhanced Configuration Access Mechanism

#### DEBUGGING A PCI EXPRESS SYSTEM

- Compliance lists
- The Serial Data Analyser from **Lecroy**, test of the physical layer
- Protocol analyser / exercicer from **Lecroy**
- Trace

analysis

### DOCUMENTATION

- Training manuals will be given to attendees during training in print.