

## MCF 5272 IMPLEMENTATION

Ref : 003281A

Duration : 3 days

### OBJECTIVES

- Optimized code writing based on pipeline knowledge
- Memory controller understanding, especially the SDRAM controller
- Explaining the operation of the Fast Ethernet controller and particularly the buffer management
- Initializing the USB interface to communicate with a host computer

### RELATED COURSES

- The course 003367A explains the operation of the **Ethernet network**
- The course 002606A explains the operation of the **USB bus**
- For programmers having to develop a BSP or a driver, the course 002603A called **C language for real time and embedded applications** is recommended

### PREREQUISITES

- Experience of a 32 bit processor or DSP is mandatory

### PARTNERS

- This training course is approved by FREESCALE



### Contact

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Course also available  
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

### TOPICS

#### THE V2 COLD FIRE CORE

- ColdFire core versions
- Pipeline basics
- Description of assembly instructions
- Mac instructions, implementation of a fixed point DFT
- ColdFire instruction set architecture enhancements
- Stack management
- C to assembly interface
- Section definition
- Exception management
- Cache basics
- 1-kB instruction cache operation
- Programming region attributes in Access Control Registers
- Internal 4-kB SRAM
- Power management

#### DEBUG FACILITIES

- Intrusive vs non-intrusive debug
- BDM port
- Hardware breakpoints
- Trace port

#### RESET

- Reset sources
- Reset control flow
- Chip mode selection
- Boot device selection
- Requirements of the boot routine

#### DEVICE CONFIGURATION

- System Control Module
- Internal bus arbitration,
- Clocking
- The interrupt controller

#### HARDWARE IMPLEMENTATION

- External bus signals
- Dynamic bus sizing
- Data transfer sequence
- Burst cycles
- External master interface

- The memory controller
- SDRAM basics
- The SDRAM controller

#### TIMERS

- Programmable Interrupt Timer Modules
- The PWM module, programming frequency and duty cycle

#### THE DMA CONTROLLER

- Dual address transfers, continuous-mode or cycle-steal transfers
- Hardware interface, hardware initiated transfers
- Burst transfers

#### COMMUNICATION CONTROLLERS

##### The 2 UARTs

- UART basics, frame format
- Line break generation
- Transmit and receive sequences

##### The QSPI

- SPI protocol basics
- Baud rate selection, transfer delays
- Command queue
- Transmit and receive sequences

##### The PLIC [Physical Layer Interface Controller]

- TDM communications basics, introduction to ISDN
- Interface with the PHY : IDL vs GCI
- Configuration of the interface
- Transmit and receive sequences

##### The USB controller

- USB protocol basics
- Endpoint initialization, FIFO management
- Data flow

##### The Fast Ethernet Controller

- Ethernet basics
- MII hardware interface
- Buffer management, buffer chaining
- Full duplex operation
- Receive and transmit sequences
- Error management

**DOCUMENTATION**

Training manuals will be given to attendees during training **both in pdf and in print**. Precise and easy to use, those notes can be used as a reference afterwards.

**CONTACT INFORMATIONS**

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