
VHDL - Language introduction

Ref : 003342A

Duration : 3 days

OBJECTIVES

- This training is directed to electronic engineers who already have a great knowledge in designing digital electronic circuits, who are willing to acquire the basis of VHDL language, in order to gain a better knowing of the possibilities in the area of logical synthesis and simulation.
- A large number of practical labs with demonstrations allows a good understanding of the basic principles, thanks to the writing of a synthesizable generic code with its associated simulation testbench that allows to check its working.

RELATED COURSES

- VHDL - Advanced design methodology (003342A)
- VHDL Logical Synthesis and Simulation for Xilinx FPGA design (002572A)

TRAINING MATERIALS

Software Configuration :

- Xilinx ISE
- Simulation tool : ISIM or Modelsim

Recommended Hardware Configuration :

- Intel Core 2 or equivalent
- Windows XP
- 1 GB Free disk after software installation
- At least 1Go RAM
- Minimum Display resolution : 1024 x 768
- On Site training : video projector

Contact

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Course also available
customized

Next sessions, see : <http://www.mvd-training.com/en/schedule.html>

TOPICS

- The Association Entity-Architecture
 - Principal rules of ports declaration
 - Internal signals declaration
 - Examples
- Frequently Manipulated Objects in Logical Synthesis
 - Signals, variables, constants
- Predefined type
 - Bit, bit_vector – limits of these types
 - Booleans
 - Integers
 - “User defines” objects
- Std_logic, Std_logic_vector and Std_logic_1164 package
 - Advantages compare to predefined types in logical synthesis and simulation
 - Interpretation by synthesizer and simulators
- Predefined Operators and their extended use to Std_logic_vector
 - Logical operators
 - Relative operators – tricks to avoid
 - Arithmetical examples
- Rules to follow for the assignment of data carriers
 - Typical examples
- Competing instructions and use rules
 - When ... else
 - With ... select
 - For generate
- Implementation of several sample designs, in order to highlight the fundamental characteristics of these instructions.
- Sequential instructions and use rules
 - If ... else
 - Case
 - For ... loop
 - Sample design, synchronous counter
 - Initializable
 - Chargeable
 - Up-down
 - Cascadable
 - Implementation of a state machine and simulation of it
 - Implementation of several sample designs, in order to highlight the fundamental characteristics of these instruction
- Initiation to VHDL Language simulation
 - A few new instructions directly linked to simulation
 - After
 - Wait for
 - Simulation of previously developed sample designs
- Management of hierarchy and structural VHDL
 - How to separate the design into interlinked modules
 - Use of Cores and IP
 - Use of specific primitives of targeted technologies and simulation of them
- Predefined attribute and notion of genericity
 - Range, reverse_range, length, left, right
 - Example of use
 - Introduction of subprograms (functions and procedures), and highlighting the use of generics
 - Implementation of hierarchical design of micro processor interface and programmable timer with interruption line

DOCUMENTATION

Training manuals will be given to attendees during training in print.