
MCF 548X IMPLEMENTATION

Ref : 003382A

Duration : 4 days

OBJECTIVES

- Optimized code writing based on pipeline knowledge
- Memory controller understanding, especially DDR SDRAM controller
- Understanding the operation of the Fast Ethernet controller
- Detailing the reset sequence
- Programming of an Interrupt Service Routine

RELATED COURSES

- The course 002601A explains the operation of the **CAN bus**
- The course 002596A explains the operation of the **PCI bus**
- The course 002606A explains the operation of the **USB bus network**
- The course 003367A explains the operation of the **Ethernet network**
- For programmers having to develop a BSP or a driver, the course 002603A called **C language for real time and embedded applications** is recommended

PREREQUISITES

- Experience of a 32 bit processor or DSP is mandatory

PARTNERS

- This training course is approved by FREESCALE



Contact

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Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

INTRODUCTION TO THE MCF548X FAMILY

- ColdFire core versions
- Architecture of a typical 548X board
- Mapping of internal resources

THE V4e COLD FIRE CORE

- Pipeline basics
- Description of assembly instructions
- Floating Point Unit description
- Mac instructions, implementation of a fixed point DFT
- ColdFire instruction set architecture enhancements
- Stack management, subroutine call and return
- C to assembly interface, organization of the stack frame
- Position dependent code vs position independent code
- Section definition
- Exception management : vector table, priority, masking, precise faults
- Memory Management Unit : translation and access control, process protection
- TLB initialization
- Cache basics
- 32-kB cache data and instruction, a four-way set associative organization
- Cache coherency and invalidation, software control
- Internal 32-kB SRAM, initialization code
- Power management

DEBUG FACILITIES

- Intrusive vs non-intrusive debug
- BDM port
- Hardware breakpoints
- Trace port

RESET

- Reset sources
- Clocking, system clock generation, PLL control, loss of clock detection
- Reset control flow
- Requirements of the boot routine

SIU & INTERRUPT CONTROLLER

- System Control Module
- Internal bus arbitration
- The interrupt controllers : vectorized vs auto-vectorized mode, edge Port Module

HARDWARE IMPLEMENTATION

- Electrical specification, supply voltage sequencing
- Flexbus
- DDR SDRAM basics
- DDR SDRAM Controller
- PCI Controller
- Error management

TIMERS

- Programmable Interrupt Timer Modules
- General Purpose Timer Modules
- Input capture capability

THE MULTI CHANNEL DMA CONTROLLER

- DMA task memory
- DMA sources
- Transfer control descriptors

COMMUNICATION CONTROLLERS

- The PSC Module
- The DSPI
- The I2C controller
- The FlexCAN controller
- The Fast Ethernet Controller
- The USB 2.0 device controller

INTEGRATED SECURITY ENGINE

- crypto-channels
- ARC four execution unit
- Multi-function data packet descriptors

DOCUMENTATION

Training manuals will be given to attendees during training **both in pdf and in print**. Precise and easy to use, those notes can be used as a reference afterwards.

CONTACT INFORMATIONS

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