

COLDFIRE 523X IMPLEMENTATION

Ref : 003440A

Duration : 4 days

OBJECTIVES

- Optimized code writing based on pipeline knowledge
- Memory controller understanding, particularly the SDRAM controller
- Detailing the reset sequence
- The interrupt controller is viewed in detail
- Implementing the Fast Ethernet controller and using the cryptography modules
- Generation of DMA transfers terminated by interrupt

RELATED COURSES

- The course 002601A explains the operation of **CAN bus**
- The course 002606A explains the operation of **USB bus**
- The course 003367A explains the operation of **Ethernet network**
- For programmers having to develop a BSP or a driver, the course 002603A called **C language for real time and embedded applications** is recommended
- The training called **TPU programming** (reference 003199A) is recommended for persons involved in development of custom TPU functions

PREREQUISITES

- Experience of a 32 bit processor or DSP is mandatory

PARTNERS

- This training course is approved by FREESCALE



Contact

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Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

INTRODUCTION TO MCF523X

- Coldfire roadmap
- 523X block diagram
- Pinout
- Memory mapped I/O organization

V2E CORE

- V2E pipeline
- Addressing modes
- Branch, data transfer, arithmetic, logic, shift & rotate, bit instructions
- Mac instructions, implementation of a fixed-point DFT
- C to assembly interface
- Section definition, parameterizing the linker command file
- Exception management
- Internal SRAM
- 523X cache operation
- Power management

DEBUG FACILITIES

- Intrusive vs non-intrusive debug
- BDM port
- Hardware breakpoints
- Trace port

RESET

- Reset sources
- Clocking
- Reset control flow
- Chip Configuration Module [CCM]
- Requirements of the boot routine

CENTRAL PERIPHERALS

- SCM
- The interrupt controller
- The Edge Port Module

- Watchdog timer module
- Programmable Interrupt Timer Modules

THE DMA CONTROLLER

- Channel prioritization
- Bandwidth control
- Transfer termination
- Utilization of DMA timers

HARDWARE IMPLEMENTATION

- Dynamic bus sizing
- Address decoding
- Data transfer sequence
- Burst cycles

THE MEMORY CONTROLLER AND THE SDRAM CONTROLLER

- The memory controller : SRAM/Flash connection, chip-select programming
- DRAM / SDRAM basics
- The 523X (S)DRAM controller : address decoding, refresh rate definition, address multiplexing selection

COMMUNICATION CONTROLLERS

- The UART Module
- The QSPI
- The I2C controller
- The FlexCAN controller
- The Fast Ethernet Controller

CRYPTOGRAPHY MODULES

- Message Digest Hardware Accelerator
- Random Number Generation
- Symmetric key hardware accelerator, introduction to data encryption standards
- Data flow, management of input and output FIFOs

DOCUMENTATION

Training manuals will be given to attendees during training **both in pdf and in print**. Precise and easy to use, those notes can be used as a reference afterwards.

CONTACT INFORMATIONS

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