

## PowerPC MPC 834X (PowerQUICC II PRO)

Ref : 003489A

Duration : 5 days

### OBJECTIVES

- The course focuses on the sequencer that interconnects e300, DDR SDRAM, PCI and external bus
- Cache coherency protocol is introduced in increasing depth
- The 32-bit e300 core is viewed in detail, especially the MMU and the cache
- The boot sequence and the clocking are explained
- The course focuses on hardware implementation of the MPC834X
- A long introduction to DDR SDRAM operation is done before studying the DDR SDRAM controller
- An in-depth description of the PCI controllers is performed
- The course highlights both hardware and software implementation of gigabit / fast / Ethernet controllers
- The USB interfaces are also detailed.

### RELATED COURSES

- USB course (Reference 002606A)
- PCI course (Reference 002596A)
- Ethernet course (Reference 003367A).

### PREREQUISITES

- Experience of a 32 bit processor or DSP is recommended

### PARTNERS

- This training course is approved by FREESCALE



WIND RIVER



NeoMore

### Contact

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Course also available  
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

### TOPICS

#### INTRODUCTION TO MPC 834X

- General features
- Enhancements compared to MPC824X
- Block diagram
- Features of the MPC8343E, MPC8347E and MPC8249E

#### THE e300 CORE

##### THE INSTRUCTION PIPELINE

- Pipeline basics
- Branch processing unit
- Branch instructions
- Simplified branch mnemonics

##### DATA PATHS

- Load / store buffers
- Sync and eieio instruction

##### CACHES

- Cache basics
- Cache locking
- L1 caches
- Cache coherency mechanism
- The MEI state machine
- Management of cache enabled pages shared with PCI DMAs
- Reservation coherency
- Cache related instructions
- Software enforced cache coherency
- Cache flush routine

##### SOFTWARE IMPLEMENTATION

- PowerPC architecture specification, the 3 books UISA, VEA and OEA
- e300 registers
- addressing modes, load / store instructions
- Integer instructions
- Rotate instructions : inserting and extracting bitfields
- IEEE754 basics, floating points numbers encoding
- The PowerPC EABI

#### THE MMU

- Thread vs process
- Introduction to real, block and segmentation / pagination translations
- Real mode restrictions
- Memory attributes and access rights definition
- Virtual space benefit, page protection through segmentation
- TLBs organization
- Pagination : PTE table organization, tablesearch algorithm
- Explanation of hash value and API field
- MMU implementation in real-time sensitive applications

#### THE EXCEPTION MECHANISM

- MSR, SPRG0-3, DAR and DSISR supervisor registers description
- Save / restore registers SRR0/SRR1, rfi instruction
- Exception management mechanism
- Requirements to allow exception nesting

#### THE DEBUG PORT

- JTAG emulation, restrictions
- Real time trace requirements
- Code instrumentation
- Hardware breakpoints

#### THE PLATFORM CONFIGURATION

##### POWER, RESET AND CLOCKING

- DC and AC electrical characteristics
- Power management control
- Reset causes
- Reset configuration words source, boot from I2C or boot from EEPROM
- PCI Host / Agent configuration, PCI1 and PCI2 arbiter configuration
- Clocking in PCI Host mode
- External clock inputs
- System PLL ratio
- Delay Locked Loop

**ADDRESS TRANSLATION AND MAPPING**

- Local memory map
- Local access windows
- Inbound and outbound windows definition

**ARBITER AND BUS MONITOR**

- External signal description
- PCI outbound window definition
- Transaction forwarding

**SEQUENCER**

- Coherent system bus overview
- Bus error detection
- Initialization sequence

**GENERAL PURPOSE INPUTS / OUTPUTS**

- Pin model
- Direction definition
- Interrupt inputs

**THE DDR MEMORY CONTROLLER**

- DDR-SDRAM operation
- Jedec specification basics, mode register initialization, bank selection and precharge
- Hardware interface
- Bank activation, read, write and precharge timing diagrams, page mode
- ECC error correction
- DDR-SDRAM controller introduction
- Initial configuration following Power-on-Reset
- Address decode
- Timing parameters programming
- Initialization routine

**LOCAL BUS CONTROLLER**

- Multiplexed 32-bit address and data transfers
- Burst support
- Dynamic bus sizing
- GPCM, UPMs and SDR SDRAM states machines

**PCI BUS INTERFACES**

- Bridge features
- Data flows : Read prefetch and write posting FIFOs
- Inbound transactions handling, Outbound transactions handling in both modes
- PCI bus arbitration
- PCI hierarchy configuration

**INTEGRATED DMA CONTROLLER**

- Priority between the 4 channels
- Support for cascading descriptor chains
- Scatter / gathering
- Selectable hardware enforced coherency
- Concurrent execution across multiple channels with programmable bandwidth control

**DOCUMENTATION**

- Training manuals will be given to attendees during training in print.

- Messaging unit
- Doorbells management

**INTEGRATED PROGRAMMABLE INTERRUPT CONTROLLER**

- Interrupt masking
- Definition of interrupt priorities
- Interrupt management, vector register
- Requirements to support nesting
- Machine check interrupts

**TIMERS**

- Software watchdog timer
- Real time clock module
- Periodic Interval Timer
- General Purpose Timers, cascaded modes, capture operation

**INTEGRATED PERIPHERALS****SECURITY ENGINE**

- Introduction to DES and 3DES algorithms
- Data packet descriptors
- Crypto channels
- Link tables

**THE ETHERNET CONTROLLERS**

- 802.3 specification fundamentals
- Address recognition, pattern matching
- MII interface
- Buffer descriptors management
- the three-speed Ethernet controllers (TSECs)
- Physical interfaces : GMII, MII, TBI or RGMII
- Buffer descriptor management
- Layer 2 acceleration accept or reject on address or pattern match
- 256-entry hash table for unicast and multicast

**THE USB 2.0 CONTROLLERS**

- Multi-port host (MPH) and dual-role (DR) module
- EHCI implementation
- UTMI / ULPI interfaces to the transceiver
- OTG support
- Dedicated DMA channels
- Endpoints configuration
- Queue Element transfer descriptor
- Management of isochronous pipes

**LOW SPEED PERIPHERALS**

- Description of the NS16450/16550 compliant Uarts
- FIFO mode
- Flow control signal management
- I2C protocol fundamentals
- Transmit and receive sequence
- SPI protocol basics
- Master vs slave operation