

OBJECTIVES

- The course explains the Serial ATA specification
- An architectural view of a SATA connection is studied

RELATED COURSES

- USB course (Reference 002606A),
- PCI course (Reference 002596A),
- Ethernet course (Reference 003367A)
- C language for real-time and embedded applications (002603A)

PREREQUISITES

- Experience of a bus is recommended
- This training is adapted to the electronics and programmers engineers confronted with the problems of the implementation of this bus

PARTNERS**Contact**

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**Course also available
customized**

Next sessions, see: <http://www.mvd-training.com/en/schedule.html>

TOPICS**ORIGINS OF THE SATA INTERFACE**

- Parallel ATA limitations
- Serial ATA roadmap
- Enhanced Integrated Drive Electronics (EIDE)
- Faster HDD access and logical block addressing (LBA)
- ATAPI for support of other peripheral devices
- Programmed Input / output, direct memory access (UDMA)

SATA ARCHITECTURE

- General overview, topology, connectivity
- Architectural layering
- Standard ATA emulation
- Flow control

TRANSPORT LAYER

- Frame and Frame Information Structure (FIS)
- Host transport states
- Device transport states

LINK LAYER

- Transmission words
- 8b/10b coding basics, clock recovery, code-group alignment
- Framing concepts
- Scrambling

DOCUMENTATION

Training manuals will be given to attendees during training in print.

- Link information :
 - The primitive

PHYSICAL LAYER

- Cable and connectors
- Electrical signaling
- Spread Spectrum Clocking
- Link initialization
- Elastic buffer
- Power and signal lines
 - OOB signals (Out Of Band)

POWER MANAGEMENT

- Interface power states
- Power management primitives
- Comwake signal sequence

HIGH LEVEL OPERATION

- Device command layer protocol
- Host adapter register interface
- Error handling

TESTING AND VERIFICATION

- Serial ATA analysers
- Traffic capture
- Test and verification of SATA devices