
Serial ATA II

Ref : 003523A

Duration : 2 days

OBJECTIVES

- Packet switching benefits compared to shared busses are highlighted

PREREQUISITES

- Experience of a high speed digital bus like PCI-X or IEEE1394 is recommended



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Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

ORIGINS OF THE SATA INTERFACE

- Parallel ATA limitations
- Serial ATA roadmap
- Enhanced Integrated Drive Electronics (EIDE)
- Faster HDD access and logical block addressing (LBA)
- ATAPI for support of other peripheral devices
- Programmed Input / output, direct memory access (UDMA)

SATA ARCHITECTURE

- General overview, topology, connectivity
- Architectural layering
- Standard ATA emulation
- Flow control

TRANSPORT LAYER

- Frame and Frame Information Structure (FIS)
- Host transport states
- Device transport states

LINK LAYER

- Transmission words
- 8b/10b coding basics, clock recovery, code-group alignment
- Framing concepts
- Scrambling

PHYSICAL LAYER

- Cable and connectors
- Electrical signalling
- Spread Spectrum Clocking
- Link initialization
- Elastic buffer
- Power and signal lines

POWER MANAGEMENT

- Interface power states
- Power management primitives
- Comwake signal sequence

HIGH LEVEL OPERATION

- Device command layer protocol
- Host adapter register interface
- Error handling

TESTING AND VERIFICATION

- Serial ATA analysers
- Traffic capture
- Test and verification of SATA devices

DOCUMENTATION

- Training manuals will be given to attendees during training in print.