
PPC 440 CORE

Ref : 003528A

Duration : 3 days

OBJECTIVES

- A boot firmware that initializes the MMU has been developed
- Internal debug facilities are described
- The course focusses on 440 low level programming, especially the PowerPC EABI
- Examples of exception handlers are provided
- A DFT has been developed to explain how to use mac instructions
- The Floating Point Unit operation is described

RELATED COURSES

- The knowledge of C language for real-time and embedded applications (course 002603A) is recommended
- In order to understand how the core communicates with peripherals, the CoreConnect course (reference 002585A) is also recommended

PREREQUISITES

- Experience of a 32 bit processor or DSP is mandatory

PARTNERS

- This training course is approved by IBM Microelectronics

Contact

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Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

INTRODUCTION TO 440

- Internal architecture overview
- Connection to peripheral IPs
- Clocking
- Programming model

THE CORE ARCHITECTURE

- Pipeline basics
- 5-stage pipeline operation
- Speculative execution, guarded memory
- Cache basics
- Data flow between external memory and caches
- Cache programming interface
- Process vs thread
- Memory Management Unit
- Translation Lookaside Buffer initialisation
- Cache control and debugging features
- Load / store buffer, speculative loads,

BOOK E COMPLIANT CORE

- Booke E objectives
- Branch instructions
- Load / store instructions
- Semaphore management with lwarx / stwcx. Instructions

- Arithmetical and logical instructions
- The PowerPC EABI
- Cache related instructions
- 16-bit mac instructions to develop fixed point DSP algorithms
- Exception processing
- Syndrome registers updating when an exception is taken
- Core timers : PIT, FIT and WDT
- Reset

INTEGRATED DEBUG FACILITIES

- JTAG emulator use
- Real time trace when the PowerPC core executes cached instructions
- Hardware vs software breakpoints

HARDWARE IMPLEMENTATION OF THE PPC440 CORE

- External connections
- Clock and power management interface
- CPU control interface
- Reset interface
- External interrupt controller interface
- Instruction-side local bus interface
- Data-side local bus interface
- DCR interface

DOCUMENTATION

Training manuals will be given to attendees during training **both in pdf and in print**. Precise and easy to use, those notes can be used as a reference afterwards.

CONTACT INFORMATIONS

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