STR7 MICROCONTROLLERS IMPLEMENTATION

Ref : 003728A **Duration : 4 days**

OBJECTIVES

- The course details the hardware implementation of the STR71x microcontrollers
- The boot sequence and the clocking are explained
- Practical labs on integrated peripherals are based on I/O functions provided by ST
- The course focuses on the low level programming of the ARM7TDMI core
- The course provides examples of internal peripheral software drivers

RELATED COURSES

- USB training (Ref.002606A)
- CAN training (Ref.002601A)
- ARM-7 / ARM-9 System Design (Ref.002879A)
- ARM Software development using RealView (Ref.002580A)
- Ethernet training (Ref.003367A)

PARTNERS

- MVD Training is a **ST MCU Certified Training Partner**
- MVD Training is an **ARM Approved Training Centre**

PREREQUISITES

- A basic understanding of microprocessors and microcontrollers is recommended
- A basic understanding of digital logic or hardware / ASIC design issues would be useful but not essential
- A basic understanding of assembler or C programming would be useful but not essential

PRACTICAL LABS

- For on-site courses, labs can be run under the following environments : Keil µVision, or IAR Workbench
- For open courses, labs are run under IAR Workbench

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Course also available customized

Next sessions, see : *http://www.mvd-fpga.com/en/formationsCalend.html*

TOPICS

INTRODUCTION TO STR71XF

- ARM core based architecture
- APB internal busses
- The main three blocks : platform, core and input / output peripherals

THE ARM7TDMI CORE

- Presentation of the core, architecture and programming model
- Operating modes : user, system, super, IRQ, FIQ, undef and abort
- Pipeline
- ALU data path
- ARM vs Thumb instruction sets, interworking
- Access to memory-mapped locations, addressing modes
- Stack management
- Branch instructions, implementation of C call and return statements
- Benefits of condition set capability in ARM state
- C-to-Assembly interface
- Exception mechanism, handler table
- Debug facilities

INFRASTRUCTURE

- APB Bridges, individual peripheral reset control, individual peripheral clock control
- Memory organization, linear 4 GB mapping
- Internal 64 kB SRAM, dynamic remapping capability
- Flash memory, bank and sector mapping, burst mode
- Program and erase sequences
- Interrupt controller
- ISR header and footer routines
- External interrupts Unit
- System timers : Real Time Clock, Watchdog timer

HARDWARE IMPLEMENTATION

- Power supplies, external 3.3V, internal generation of 1.8V, related pins
- Low voltage detectors
- Clocking
- Reset causes
- Start-up sequence, fetch of the first instruction
- Boot configuration register
- Low power modes
- External Memory Interface
- Description of the programming interface related to the 4 external chip-selects

TIMERS

- 16-bit timers, block diagram, clock selection and prescalers
- Output compare and input capture capabilities, force compare modes
- Output PWM mode, on-the-fly modification of the duty cycle
- Input PWM mode, pulse measurement

ANALOG-TO-DIGITAL CONVERTER

- High impedance-analog input configuration
- ADC features : 12-bit resolution, 0 to 2.5 V range
- Round-robin or single channel mode
- Clock timing
- The Sinc decimation filter
- Gain and offset errors

I2C INTERFACE

- I2C protocol basics
- Slave mode vs master mode
- Transmit and receive sequences

BUFFERED SPI

- SPI protocol basics
- Queue mode operation

- Transfer sequence

UART

- Queue operation mode
- Time-out mechanism
- SmartCard asynchronous protocol

CAN CONTROLLER

- CAN protocol basics
- CAN controller organization
- Message objects
- Filtering received messages
- FIFO mode management
- Configuring the bit timing

USB SLAVE INTERFACE

- USB protocol basics
- Buffer description block, buffer descriptor table
- Double buffer usage to support isochronous and high throughput bulk transfers
- Endpoint initialization

HDLC CONTROLLER

- HDLC protocol basics
- Address decode
- DPLL use for clock recovery
- Abort sequence generation
- Transmit and receive sequencesTitle 1

DOCUMENTATION

Training manuals will be given to attendees during training in print.