
Designing with PlanAhead

Ref : 004088A

Duration : 2 days

OBJECTIVES

- Learn to increase design performance and achieve repeatable results by using the PlanAhead™ tool
- Learn the PlanAhead tool features and benefits
- Import a design into the PlanAhead tool project environment
- Optimized planing constraint application for IOs
- Import HDL source and analyze the generated netlist
- Implement the design with different implementation strategies
- Analyze design statistics, connectivity, timing and placement
- Design Rule Checker (DRC) and Weighted Average SSO analysis
- Insert ChipScope cores

RELATED COURSES

- Designing for performance, ISE (002833A)
- Designing with the Virtex-5 Family (004555A)
- Virtex 6, ISE 11 (004852A)
- Spartan 6, ISE 11 (004851A)

PARTNERS

- This training course is approved by XILINX

PREREQUISITES

- Good experience on the ISE tool
- Several Xilinx FPGAs designed

TRAINING MATERIALS

Software Configuration :

- Xilinx ISE Design Suite 11.1 Logic Edition

Recommended Hardware Configuration :

- Intel Core 2 or equivalent
- Windows XP
- 1 GB Free disk after software installation
- At least 1Go RAM
- Minimum Display resolution : 1024 x 768
- On Site training : video projector

Authorized
Training Provider

Contact

Tel : 05 62 13 52 32
Fax : 05 61 06 72 60
training@mvd-fpga.comCourse also available
customized

Next sessions, see : <http://www.mvd-training.com/en/schedule.html>

TOPICS

1st Day

- Introduction
 - PlanAhead Tool Benefits
 - PlanAhead Tool Features
 - PlanAhead Tool Design Flow
 - Creating a Project
 - Exercise : Getting started with the PlanAhead tool
- I/O pin and clock planning
 - Using the PinAhead Environment
 - Importing and Analyzing an I/O Port List
 - Creating and Configuring I/O Ports
 - Creating I/O Port Interfaces
 - Selecting Alternate Compatible Parts
 - Placing I/O Ports
 - Running DRC and WASSO Analysis
 - Exporting an I/O Port List
 - Exercise
- RTL Development and analysis
 - Importing and Managing RTL Sources
 - Using the HDL Editor
 - Elaborating the RTL Design
 - Exploring the Logic Hierarchy
 - Viewing the RTL Schematic
 - Analyzing Resource Estimates
 - Running RTL DRCs
 - Exercise
- Implementing a design
 - Synthesizing the Design
 - Implementing the Design
 - Analyzing the Results

- Creating a Bitstream file
- Creating Multiple Runs
- Exercise

2nd Day

- Design analysis
 - Device Resources and Design Statistics
 - Design Rule Checker (DRC)
 - Timing Analysis and Results Viewer
 - Viewing and Modifying Constraints
 - Analyzing Placement Results
 - Design Utilization and Timing Metrics
 - Search Capabilities Using Find
 - Logic Connectivity Analysis
 - Exercise
- Floorplanning techniques
 - Why Floorplan?
 - Floorplanning Tips
 - Block-Based Design Techniques
 - Floorplanning Primitives
 - Maximizing Density
 - Exercise
- Debugging with the ChipScope tool
 - ChipScope Pro Tool Integration
 - Selecting Signals for Debugging
 - Configuring ChipScope Pro Tool Cores
 - Implementing ChipScope Pro Tool Cores
 - Launching the ChipScope Pro Analyzer
 - Exercise
- Project Navigator Integration with the PlanAhead Tool
 - Exercise

DOCUMENTATION

Training manuals will be given to attendees during training in print.