

Designing with PlanAhead

Ref : 004088A

Duration : 3 days

OBJECTIVES

- Know the PlanAhead™ tool features and benefits
- Create project and import sources (HDL, netlist) into the PlanAhead tool project environment
- Instantiate a core from the Xilinx IP Catalog and insert ChipScope™ Pro tool debug cores
- Elaborate HDL sources and analyze RTL netlists
- Implement the design with different synthesis and implementation strategies
- Assign I/O pins for optimum speed
- Run the Design Rule Checker (DRC) and perform noise analysis
- Apply the hierarchical viewer and timing report information to make the best area constraints
- Group the best logic into Pblocks
- Floorplan the design to improve performance and preserve successful implementation results
- Analyze design statistics, connectivity, timing, placement, and timing critical paths
- Make placement constraints for dedicated hardware resources

RELATED COURSES

- Designing for performance, ISE (002833A)
- Advanced FPGA Implementation (002824A)
- Virtex 6, ISE (004852A)
- Spartan 6, ISE (004851A)

PARTNERS

- This training course is approved by XILINX

PREREQUISITES

- Good experience on the ISE tool
- Several Xilinx FPGAs designed

TRAINING MATERIALS

Software Configuration :

- Xilinx ISE Design Suite 13.1 Logic Edition

Recommended Hardware Configuration :

- Intel Core 2 or more recent
- Windows XP or 7
- 1 GB Free disk after software installation
- At least 2Go RAM
- Minimum Display resolution : 1024 x 768
- On Site training : video projector

Authorized
Training Provider

Contact

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Course also available
customized on site

Next sessions, see : <http://www.mvd-training.com/en/schedule.html>

TOPICS

1st Day

- PlanAhead Tool Benefits and Features overview
- PlanAhead Tool Project manager
 - PlanAhead Tool Design Flows
 - Creating a Project
 - Project Manager
 - PlanAhead Software Tips
 - Lab 1: Getting started with the PlanAhead tool
- I/O pin planning
 - Using the Pin Planning Environment
 - I/O layout
 - Importing and Exporting I/O Port List
 - Creating, Configuring and Placing I/O Ports and Interfaces
 - Running DRC and noise Analysis
 - Selecting Alternate Compatible Parts
 - Lab 2: Assign I/O Pins
- CoreGenerator Tool Integration
 - Lab 3: Core Integration
- Static Timing Analysis with the PlanAhead Software
 - Static Timing estimation with TimeAhead
 - Static Timing Analysis with Sign-Off quality Timing Information
- Project Navigator integration with the PlanAhead Software

2nd Day

- RTL Development and Analysis
 - Exploring the logic Hierarchy
 - Viewing the RTL Schematic
 - Analyzing Resource Estimates
 - Netlist Timing Analysis

- Lab 4: RTL analysis
- Placing Dedicated Resources
 - What is Floorplanning?
 - Making Placement Constraints
 - Lab 5: Placing Dedicated Resources
- Pblocks
 - Why Floorplan?
 - Design and Synthesis Recommendations
 - Pblocks and Floorplanning Tools

3rd Day

- Floorplanning Techniques
 - Floorplanning Principles
 - Floorplanning Methodologies
 - Lab 6: Design Analysis and Floorplanning for Performance
- Design Preservation with Partitions
 - Lab 7: Design Preservation for Predictable Results
- Debugging with the ChipScope Pro Tool
 - Lab 8: Debugging with the ChipScope Pro Tool
- Tcl Scripting in the PlanAhead Software
 - Basics of Tcl
 - Tcl in the PlanAhead Software
 - PlanAhead Software-Specific Commands
 - Lab 9: Tcl Commands
- Team Design *
 - Team-Based Design Setup
 - Hierarchical Design Considerations
- Routing Optimization in Virtex-6 Devices *
 - Diagnosing a Routing Problem
 - HDL Coding Styles to Improve Your Routing Solution
 - How to Achieve Routing Optimization

*Optional parts that need extra time

DOCUMENTATION

Training manuals will be given to attendees during training in print.