STR9 MICROCONTROLLERS IMPLEMENTATION

Ref : 004337A **Duration : 4 days**

OBJECTIVES

- The course details the hardware implementation of the STR91x microcontrollers
- The boot sequence and the clocking are explained
- The course focuses on the low level programming of the ARM966 CPU
- Practical labs on integrated peripherals are based on I/O functions provided by ST

RELATED COURSES

- USB training (Ref.002606A)
- CAN training (Ref.002601A)
- Ethernet training (Ref.003367A)
- ARM-7 / ARM-9 System Design (Ref.002879A)
- ARM Software development using RealView (Ref.002580A)

PARTNERS

- MVD Training is a **ST MCU Certified Training Partner**
- MVD Training is an **ARM Approved Training Centre**

PREREQUISITES

- A basic understanding of microprocessors and microcontrollers is recommended
- A basic understanding of digital logic or hardware / ASIC design issues would be useful but not essential
- A basic understanding of assembler or C programming would be useful but not essential

PRACTICAL LABS

- For on-site courses, labs can be run under the following environments : Keil µVision, or IAR Workbench
- For open courses, labs are run under IAR Workbench

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Course also available customized

Next sessions, see : *http://www.mvd-fpga.com/en/formationsCalend.html*

TOPICS

INTRODUCTION TO STR91XF

- ARM core based architecture
- Features of AHB and APB buses
- The main three blocks : platform, core and input / output peripherals

THE ARM966E-S CPU

- Operating modes : user, system, super, IRQ, FIQ, undef and abort
- Pipeline, calculation of the CPI
- Branch cache
- Clarifying the data path
- Tightly Coupled Memories
- ARM vs Thumb instruction sets, interworking
- Stack management
- Benefits of condition set capability in ARM state
- C-to-Assembly interface
- Exception mechanism, handler table
- Debug facilities

INFRASTRUCTURE

- AHB/APB Bridges, split transactions, error handling
- Internal 96 KB SRAM,
- Flash memory
- Program and erase sequences
- VIC Interrupt controller
- Wake-up / interrupt unit
- System timers : Real Time Clock, Watchdog timer

HARDWARE IMPLEMENTATION

- Low voltage detectors
- Clocking
- Reset causes
- Start-up sequence, fetch of the first instruction
- Low power modes
- External Memory Interface
- I/O Ports

TIMERS

- Output compare and input capture capabilities, force compare modes
- One pulse mode
- Output PWM mode, on-the-fly modification of the duty cycle
- Input PWM mode, pulse measurement

DMA CONTROLLER

- Request priority management between the 16 channels
- Scatter / gather operation, transfer descriptor chaining
- Error management

ANALOG-TO-DIGITAL CONVERTER

- One-shot or continuous conversion
- Analog watchdog with interrupt generation

3-PHASE INDUCTION MOTOR CONTROLLER

- Tacho counter operating modes
- Rotor speed measurement
- Dead time generator

I2C INTERFACE

- I2C protocol basics
- Slave mode vs master mode
- Support for DMA

SYNCHRONOUS SERIAL PERIPHERAL [SSP]

- SPI protocol basics
- Queue mode operation
- Transfer sequence

UART

- Queue operation mode
- Hardware flow control
- IrDA mode
- Support for DMA

CAN CONTROLLER

- CAN protocol basics
- CAN controller organization
- Message objects
- Filtering of received messages
- FIFO mode management

USB SLAVE INTERFACE

- USB protocol basics
- Buffer description block, buffer descriptor table
- DMA controller used to move data between buffers and EndPoints
- Endpoint initialization

FAST ETHERNET CONTROLLER

- 802.3 MAC basics
- Connection to the PHY : MII bus
- Management interface, auto-negotiation
- DMA controller operation
- Frame filtering
- VLAN support
- Error managementTitle 1

DOCUMENTATION

Training manuals will be given to attendees during training in print.