

Designing a LogiCore PCI Express system

Ref : 004552A

Duration : 2 days

OBJECTIVES

- This course focuses on the Xilinx LogiCore PCI Express usage to develop PCI-Express based system
- Understand PCI-e specification and architectures
- Use the Xilinx flow when using LogiCore PCI-e
- Understand the features of the LogiCore PCI-e
- Use the LogiCore PCI-e in your own development environment
- Choose the appropriate PCI-e solution for a given application
- Identify how PCI-e specification apply to the LogiCore PCI-e
- This course targets Spartan-6 and Virtex-6 Xilinx FPGAs

RELATED COURSES

- PCI 3.0 Standard (002596A)
- PCI-X 2.0 Standard (002597A)
- PCI-Express Standard (003279A)
- Designing a LogiCore PCI-X System (002842A)
- Designing a LogiCore PCI System (002841A)

PARTNERS

- This training course is approved by XILINX

PREREQUISITES

- Working experience with ISE
- Intermediate knowledge of VHDL
- Basic knowledge of PCI-Express standard or very good knowledge of PCI or PCI-X standard

TRAINING MATERIALS

Software Configuration :

- Xilinx ISE Design Suite 11.4 Logic Edition

Recommended Hardware Configuration :

- Intel Core 2 or equivalent
- Windows XP
- 1 GB Free disk after software installation
- At least 1Go RAM
- Minimum Display resolution : 1024 x 768
- On Site training : video projector



Contact

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Course also available
customized

Next sessions, see : <http://www.mvd-training.com/en/schedule.html>

TOPICS

1st day

- Introduction to the PCIe Architecture
 - Overview and Architecture
 - Protocol and basics
 - Performance
- Review of the PCIe protocol
 - Transaction types and categories
 - Address space map and Configuration Space
- PCIe and Core Generator
 - Core Selection
 - Configuration Space
- Lab1 : Construction the PCIe Core
- Simulating a PCIe Design
 - Identifying Simulation Points
 - Simulation methods
 - Building testbenches
- Connecting logic to the core – LocalLink
 - PCIe Link and System Interface Signals
 - Common Transaction Interface Signals
 - Transmit examples
 - Receive examples
 - Configuration Space examples
- Memory Read and Memory Write Completion details
 - Introduction
 - MemW

- MemR
- CplD
- Lab 2 : Downstream port Model Simulation
 - endpoint application considerations
 - Design specifications and considerations
 - Selecting the appropriate Core
 - Specific Register Awareness
 - Endpoint responsibilities
- Lab 3 : Pseudo-transactional modeling

2nd day

- Application Focus : DMA
- Lab 4 : Design Implementation
 - Virtex 6 FPGA root port
 - Root port
 - Core Selection
 - Compliance and Debugging
 - Chipscope Pro tool and Debugging a PCIe Core Endpoint
 - Compliance Testing
 - Tools Required
- Lab 5 : Debugging the PCIe Core with Chipscope Pro Tools
- Errors and interrupts
 - PCIe errors
 - Advanced error reporting
 - Interrupts

DOCUMENTATION

Training manuals will be given to attendees during training in print.