

Designing a LogiCore PCI Express system

Ref : 004552A
Duration : 2 days

OBJECTIVES

- This course focuses on the Xilinx LogiCore PCI Express usage to develop PCI-Express based system
- Understand PCI-e specification and architectures
- Use the Xilinx flow when using LogiCore PCI-e
- Understand the features of the LogiCore PCI-e
- Use the LogiCore PCI-e in your own development environment
- Identify how PCI-e specification apply to the LogiCore PCI-e
- This course targets Spartan-6 and Virtex-6 Xilinx FPGAs

RELATED COURSES

- PCI 3.0 Standard (002596A)
- PCI-X 2.0 Standard (002597A)
- PCI-Express Standard (003279A)
- Spartan™-6, ISE (004851A)
- Virtex™-6, ISE (004852A)

PARTNERS

- This training course is approved by XILINX

PREREQUISITES

- Working experience with ISE
- Intermediate knowledge of VHDL
- Basic knowledge of PCI-Express standard or very good knowledge of PCI or PCI-X standard

TRAINING MATERIALS

Software Configuration :

- Xilinx ISE Design Suite 13.1 Logic Edition

Recommended Hardware Configuration :

- Intel Core 2 or more recent
- Windows XP or 7
- 1 GB Free disk after software installation
- At least 2Go RAM
- Minimum Display resolution : 1024 x 768
- On Site training : video projector

Contact

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Course also available
 customized on site


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 Training Provider

Next sessions, see : <http://www.mvd-training.com/en/schedule.html>

TOPICS

1st day

- Introduction to the PCIe Architecture
 - Overview and Architecture
 - Protocol basics
 - Performance
- Review of the PCIe protocol
 - Transaction types and categories
 - Virtual Channels and Flow Control
 - Address space map and Configuration Space
- PCIe and Core Generator
 - Core Selection
 - Configuration Space
- Lab : Construction the PCIe Core
- Simulating a PCIe Design
 - Identifying Simulation Points
 - Simulation methods
 - Building testbenches
- Connecting logic to the core – AXI Interface
 - Introduction to AXI
 - PCIe Link and System Interface Signals
 - Common Transaction Interface Signals
 - Transmit Interface Signals
 - Receive Interface Signals
 - Configuration Space Interface Signals
 - Physical Layer Interface Signals
- Packet Formatting Details
 - General TLP Format

- MemW
- MemR
- Cpl/CplD
- Msg/MsgD
- Lab : Downstream port Model Simulation
- Endpoint application considerations
 - Design specification and considerations
 - Selecting the appropriate Core
 - Specific Register Awareness
 - Endpoint responsibilities
- Lab : Pseudo-transactional modeling

2nd day

- Application Focus : DMA
- Lab : Design Implementation
- Virtex 6 FPGA root port
 - Root port
 - Core Selection
- Compliance and Debugging
 - Chipscope Pro tool and Debugging a PCIe Core Endpoint
 - Compliance Testing
 - Tools Required
- Lab : Debugging the PCIe Core with Chipscope Pro Tools
- Errors and interrupts
 - PCIe errors
 - Advanced error reporting
 - Interrupts

DOCUMENTATION

Training manuals will be given to attendees during training in print.