
Designing with the Virtex-5 Family

Ref : 004555A

Duration : 2 days

OBJECTIVES

- Learn the improvements on the Virtex-5 family compared with the Virtex-4
- Using global and area clock resources
- Using DCM and PLL
- Using memory blocks and fifo
- Using DSP48E blocks
- Understanding the new CLB
- Using source synchronous resources
- Differences between sub-families (SXT, LXT, ...)

RELATED COURSES

- VHDL logical synthesis and simulation for Xilinx FPGAs design (002572A)
- Designing for performance, ISE (002833A)
- Virtex PowerPC system implementation (002952A)
- Designing with Ethernet MAC controllers (004553A)
- Designing with Multi-Gigabit Rocket-IO transceivers (002843A)

PARTNERS

- This training course is approved by XILINX

PREREQUISITES

- Knowledge of Virtex-4 architecture
- Intermediate knowledge of ISE tool and of timing constraints.
- Intermediate knowledge of VHDL language

PRACTICAL LABS

Software configuration:

- Xilinx ISE Design Suite 11.1 Logic Edition

Recommended Hardware Configuration:

- Intel Core 2 or equivalent
- Windows XP
- 1 GB available on hard drive after software install
- At least 1GB of RAM
- Display Resolution : at least 1024 x 768
- For on site training, we need a video projector



Contact

Tel : 05 62 13 52 32
Fax : 05 61 06 72 60
training@mvd-fpga.com

Course also available
customized

Next sessions, see: <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

- Introduction
- Virtex-5 architecture overview
 - Introduction
 - Architecture improvement
- New CLB
 - Introduction
 - LUT-6 with 2 outputs
- Clock resources
 - CMT block
 - Clock network
- Exercise : Clocks management
- Inputs/Outputs
 - ChipSync technology
- Memory resources
 - Block RAM
 - FiFo
- XtremeDSP resources
 - DSP48E functionalities
 - Examples
 - Software support
- Exercise : DSP48E
- Sub-families overview

DOCUMENTATION

Training manuals in print will be given to attendees during training.