ARM CORTEX-M3 SYSTEM DESIGN

Ref : 004581A **Duration : 4 days**

OBJECTIVES

- This course takes an in depth look at the considerations you will need to take into account when designing a system containing a Cortex-M3 processor core
- It is aimed at :
  - Software engineers who not only want to obtain details of how to write software to run on the Cortex-M3, but also wish to obtain an understanding of hardware design issues
  - Hardware engineers who need to understand how to design Cortex-M3 based systems, but also wish to obtain an understanding of the issues of writing software to run on that system

RELATED COURSES

- ARM-7 / ARM-9 System Design (Ref.002879A)
- C language for embedded and real time applications (Ref.002603A)

PARTNERS

- This training course is approved by ARM

PREREQUISITES

- A basic understanding of microprocessors and microcontrollers is recommended
- A basic understanding of digital logic or hardware / ASIC design issues would be useful but not essential
- A basic understanding of assembler or C programming would be useful but not essential
- A basic awareness ARM cores is useful but not essential

PRACTICAL LABS

- For on-site courses, labs can be run under the following environments : Eclipse/RVDS, Keil µVision, GNU/Lauterbach simulator, or IAR Workbench
- For open courses, labs are run under Eclipse/RVDS

APPROVED TRAINING CENTRE ARM

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Course also available customized

Next sessions, see : *http://www.mvd-fpga.com/en/formationsCalend.html*

TOPICS

ARM Cortex-M3 CORPORATE INTRODUCTION

- ARM architectural summary
- Architecture challenge, meeting the challenge with profiles
- ARM instruction set evolution

ARM Cortex-M3 INTRODUCTION

- Programmer's model
- Fixed memory map
- Privilege, modes and stacks
- Memory Protection Unit
- Interrupt handling
- Nested Vectored Interrupt Controller [NVIC]
- Power management
- Debug

DEVELOPMENT TOOLS OVERVIEW

- RVCT compilation tools
- Codewarrior for RVDS
- RVD debugger
- RVISS simulator
- JTAG run control unit
- Trace capture unit

ARM Cortex-M3 CORE

- Datapath and pipeline
- Write buffer
- Bit-banding
- System timer
- State, privilege and stacks
- System control block

THUMB-2 INSTRUCTION SET

- Data processing instructions
- Branch and control flow instructions
- Memory access instructions
- Exception generating instructions
- If…then conditional blocks
- Exclusive load and store instructions
- Accessing special registers
- Memory barriers and synchronization
- Workbook : introductory tutorial for Cortex-M3

INTERRUPTS

- Interrupt entry / exit, timing diagrams
- Tail chaining
- Interrupt response, pre-emption
- Interrupt prioritization
- Interrupt implementation configurability, impact on core size

EXCEPTIONS

- Exception behavior, exception return
- Non-maskable exceptions
- Privilege, modes and stacks
- Fault escalation
- Vector table

MEMORY TYPES

- Memory types, restriction regarding load / store multiple
- Device and normal memory ordering
- Access order
- Memory barriers

MEMORY PROTECTION UNIT

- Memory protection overview, ARM v7 PMSA
- Cortex-M3 MPU and bus faults
- Region overview, memory type and access control, sub-regions

- Setting up the MPU

EMBEDDED SOFTWARE DEVELOPMENT WITH Cortex-M3

- Placing code, data, stack and heap in the memory map, scatterloading
- Tailoring the C library to your target
- Reset and initialisation
- Building and debugging your image
- Long branch veneers
- Workbook : Retargeting the standard C library functions, handling interrupts

INVASIVE DEBUG

- Cortex-M3 debug features
- Monitor mode
- Flash patch and breakpoint features
- Data watchpoint and trace
- DWT registers
- AHB-Access Port

NON-INVASIVE DEBUG

- Basic ETM operation
- ITM stimulus port registers
- DWT trace packets
- Time-stamping packets
- TPIU components
- Serial Wire connection

C/C++ COMPILER HINTS AND TIPS FOR Cortex-M3

- ARM compiler optimisations
- Mixing C/C++ and assembly
- Coding with ARM compiler
- Measuring stack usage
- Local and global data issues, alignment of structures

AMBA3.0 INTERCONNECT SPECIFICATION

- Purpose of this specification
- Example of SoC based on AMBA specification
- Differences between AMBA2.0 and AMBA3.0

AHB - ADVANCED HIGH PERFORMANCE BUS

- Centralized address decoding
- Address gating logic
- Arbitration, bus parking
- Single-data transactions
- Sequential transfers
- Retry response
- Split response
- AHB-lite specification

APB - ADVANCED PERIPHERAL BUS

- Read timing diagram
- Write timing diagram
- Operation of the AHB-to-APB bridge
- APB3.0 new features

AHB CORTEX-M3 HARDWARE IMPLEMENTATION

- Clocking and reset
- Bus interfaces , AMBA-3 compliance
- Debug interface, AHB-AP programming interface, ITM, ETM
- Connection to the TPIU

DOCUMENTATION

Training manuals will be given to attendees during training in print.