

MPC 8313E IMPLEMENTATION

Ref : 004689A

Duration : 5 days

OBJECTIVES

- The course focuses on the sequencer that interconnects e300, DDR SDRAM, PCI and external bus
- Cache coherency protocol is introduced in increasing depth
- The 32-bit e300 core is viewed in detail, especially the MMU and the cache
- The boot sequence and the clocking are explained
- The course focuses on hardware implementation of the MPC8313E
- A long introduction to DDR SDRAM operation is done before studying the DDR2 SDRAM controller
- An in-depth description of the PCI controllers is performed
- The course highlights both hardware and software implementation of gigabit / fast / Ethernet controllers
- The USB interfaces are also detailed.

RELATED COURSES

- USB course (Reference 002606A)
- PCI course (Reference 002596A)
- Ethernet course (Reference 003367A).

PREREQUISITES

- Experience of a 32 bit processor or DSP is recommended

PARTNERS

- This training course is approved by FREESCALE

**WIND RIVER****NeoMore**

Contact

Tel : 05 62 13 52 32
Fax : 05 61 06 72 60
training@mvd-fpga.com

Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

INTRODUCTION TO MPC8313E

- Enhancements compared to MPC824X
- Memory map
- Block diagram
- Application examples

THE e300 CORE

THE INSTRUCTION PIPELINE

- Pipeline
- Branch processing unit
- Simplified branch mnemonics
- Coding guidelines

DATA PATHS

- Load / store buffers
- Sync and eieio instructions
- Store gathering mechanism

CACHES

- Cache basics
- Relationship between cache and burst, critical word first order
- L1 caches
- Shared resource management
- Cache coherency mechanism
- Management of cache enabled pages shared with PCI DMAs
- Cache related instructions
- Cache flush routine

SOFTWARE IMPLEMENTATION

- PowerPC architecture specification, the 3 books UISA, VEA and OEA
- addressing modes, load / store instructions
- Integer instructions
- Rotate instructions : inserting and extracting bitfields
- IEEE754 basics, floating points numbers encoding
- Floating point arithmetical instructions
- The PowerPC EABI

- Linking an application with Diab Data, parameterizing the linker command file

THE MMU

- Thread vs process
- Introduction to real mode, block and segmentation / pagination translations
- Real mode restrictions
- Memory attributes and access rights definition
- Virtual space benefit, page protection through segmentation
- TLBs organization
- PTE table organization, tablesearch algorithm
- MMU implementation in real-time sensitive applications

THE EXCEPTION MECHANISM

- Save / restore registers SRR0/SRR1, rfi instruction
- Exception management mechanism
- Registers updating according to the exception cause
- Requirements to allow exception nesting

THE DEBUG PORT

- JTAG emulation, restrictions
- Code instrumentation
- Hardware breakpoints

THE PLATFORM CONFIGURATION

POWER, RESET AND CLOCKING

- DC and AC electrical characteristics
- Reset causes
- Configuration signals sampled at reset
- Reset configuration words source, boot from I2C or boot from EEPROM
- PCI Host / Agent configuration
- Clocking in PCI Host mode, system clock domains
- System PLL ratio
- Delay Locked Loop

ADDRESS TRANSLATION AND MAPPING

- Local memory map
- Local access windows

- Distinguishing Local Access Windows from other mapping functions
- Inbound and outbound windows definition

ARBITER AND BUS MONITOR

- External signal description
- PCI outbound window definition
- Transaction forwarding

SEQUENCER

- Coherent system bus overview
- Arbitration policy
- Bus error detection

GENERAL PURPOSE INPUTS / OUTPUTS

- Pin model
- Interrupt inputs

THE DDR2 MEMORY CONTROLLER

- DDR-SDRAM operation : a 128-Mbits DDR-SDRAM from Micron is used as an example
- Jedec specification basics
- Differences between DDR1 and DDR2
- Command truth table
- Refresh types
- Bank activation, read, write and precharge timing diagrams, page mode
- ECC error correction
- DDR-SDRAM controller overview
- Initial configuration following Power-on-Reset
- Address decode
- Timing parameters programming
- Initialization routine

LOCAL BUS CONTROLLER

- Multiplexed or non-multiplexed address and data buses
- Dynamic bus sizing
- GPCM, UPMs states machines
- Interfacing to ZBT SRAMs
- Interfacing to DSP host ports
- NAND flash controller

PCI BUS INTERFACE

- Bridge features
- Data flows : Read prefetch and write posting FIFOs
- Inbound transactions handling, Outbound transactions handling
- PCI bus arbitration
- PCI hierarchy configuration when operating as host

INTEGRATED DMA CONTROLLER

- Priority between the 4 channels
- Support for cascading descriptor chains

DOCUMENTATION

- Training manuals will be given to attendees during training in print.

- Concurrent execution across multiple channels with programmable bandwidth control
- Messaging unit
- Doorbells management

INTEGRATED PROGRAMMABLE INTERRUPT CONTROLLER

- Interrupt masking
- Definition of interrupt priorities
- System critical interrupt
- Requirements to support nesting

TIMERS

- Software watchdog timer
- Real time clock module
- Periodic Interval Timer
- General Purpose Timers

INTEGRATED PERIPHERALS

SECURITY ENGINE [optional, MPC8313E only]

- Overview of the encryption mechanism
- Introduction to DES and 3DES algorithms
- Data packet descriptors
- Crypto channels

THE ETHERNET CONTROLLERS

- 802.3 specification fundamentals
- MAC address recognition, 256-entry hash table for unicast and multicast
- Interface with the PHY (SGMII)
- Buffer descriptors management
- Flow control
- Level 2, 3 and 4 hardware acceleration mechanisms (TCP/IP Offload Engine)
- Quality of service support
- Hardware assist for IEEE1588 support

THE USB 2.0 CONTROLLER

- Dual-role (DR) operation
- EHCI implementation
- UTMI / ULPI interfaces to the transceiver
- OTG support
- Dedicated DMA channels
- Endpoints configuration

LOW SPEED PERIPHERALS

- Description of the NS16450/16550 compliant Uarts
- Flow control signal management
- I2C protocol fundamentals
- Transmit and receive sequence
- SPI protocol basics
 - Master vs slave operation