ARM RVDS TRACE AND SIMULATION

Ref : 004693A **Duration : 1 days**

OBJECTIVES

- This course provides an detailed description of the features supported by the RealView Debugger : simulation and trace
- A lot of exercices have been developed to understand the capabilities offered by these tools

RELATED COURSES

- ARM-7 / ARM-9 System Design (Ref.002879A)
- ARM-7 / ARM-9 Software Design (Ref.002580A)

PARTNERS

- This training course is approved by ARM

PREREQUISITES

- A basic understanding of microprocessors and microcontrollers is recommanded
- A basic understanding of assembler or C programming would be useful but not essential
- A basic awareness ARM cores is useful but not essential

PRACTICAL LABS

- For on-site courses, labs can be run under the following environments : CodeWarrior/ADS/AXD, Eclipse/RVDS, Keil µVision, GNU/Lauterbach simulator, or IAR Workbench
- For open courses, labs are run under Eclipse/RVDS

APPROVED TRAINING CENTRE ARM

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Course also available customized

Next sessions, see : *http://www.mvd-fpga.com/en/formationsCalend.html*

TOPICS

CONTROLLING EXECUTION WITH RVD

- The Real-View Debugger environment
- Taking control over a particular target in a multi-target system
- Loading images and binaries
- Mapping target memories
- Changing the execution context
- Debugging with command scripts
- Using macros for debugging
- Configuring workspace settings, how to configure, save and load a board package

SIMULATION WITH RVISS

- RVISS components, processor model, memory model
- Tracer, debugging support for tracing, interpreting trace file output, configuring tracer
- Profiler, configuring the profiler, RVISS cycle types, uncached cores, cached cores, page-table module
- Memory modelling with mapfiles
- Developing peripheral models
- Clarifying ISS variables like $statistics and $clock
- How to customize/modify ARM ISS to add new behavior
- Target configuration (memory features : wait states), cache size

REAL-TIME TRACE WITH ARM TOOLS

- Introduction to tracing
- Tracing with RVD commands
- How to activate / configure an instruction trace
- Setting up new trace conditions on a running core
- Configuring the conditions for trace capture, capturing trace with tracepoints
- Configuring the ETM
- Analyzing trace information, profiling trace information

DOCUMENTATION

Training manuals will be given to attendees during training in print.