
IEEE1588

Ref : 004701A

Duration : 1 day

OBJECTIVES

- The course explains the IEEE1588 standard and details some implementation solutions
- The BMC algorithm is described
- The course emphasizes the way to implement IEEE1588 on an Ethernet system and highlights the boundary between software and hardware

PREREQUISITES

- Knowledge of Ethernet is recommended

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Course also available
customized

RELATED COURSES

- Ethernet (003367A)

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS**INTRODUCTION**

- Objectives of the standard
- The need for synchronization
- Definitions

PTP CLOCK SYNCHRONIZATION MODEL

- The PTP messages
- PTP systems, acyclic graph structure
- Message filtering
- Clock properties, stratum, identifier
- Subdomain properties

PTP PROTOCOL SPECIFICATION

- Model of a subdomain of PTP clocks
- State behavior of clocks
- Protocol engine state machine
- Clock data sets, initialisation properties
- Messaging and internal event behavior of clocks

- Sync-event time-out mechanism
- Synchronization changes of the local clock
- Best Master Clock algorithm
- Clock variance computation
- Local clock synchronization
- Physical requirements for PTP implementations
- Management messages

ETHERNET IMPLEMENTATION OF PTP

- Ethernet frame type
- IP header and multicast addresses
- UDP header, assigned port numbers
- UDP payload, organization of PTP messages

FREESCALE IMPLEMENTATION OF PTP

- eTSEC Ethernet MAC
- Time-stamping
- Clock correction
- Trigger inputs
- Alarms

DOCUMENTATION

- Training manuals will be given to attendees during training in print.