i.MX27 IMPLEMENTATION + LTIB

Ref : 004731A **Duration : 4 days**

OBJECTIVES

- The course details the hardware implementation of the i.MX27 microcontroller
- The boot sequence and the clocking are explained
- The course explains all parameters that affect the performance of the system in order to easily perform the final tuning
- A description of all internal peripherals is provided
- An overview of the ARM926EJ-S core helps to understand issues caused by cache and MMU
- The course ends with practical labs explaining how to generate a Linux image as well as a Root File System, by using a tool called LTIB [Linux Target Image Builder]

RELATED COURSES

- USB training (Ref.002606A)
- CAN training (Ref.002601A)
- Ethernet training (Ref.003367A)
- ARM-7 / ARM-9 System Design (Ref.002879A)
- ARM Software development using RealView (Ref.002580A)

PARTNERS

- MVD Training is a Freescale Alliance Member
- MVD Training's Freescale related courses are approved by Freescale

PREREQUISITES

- A basic understanding of microprocessors and microcontrollers is recommended
- A basic understanding of digital logic or hardware / ASIC design issues would be useful but not essential
- A basic understanding of assembler or C programming would be useful but not essential

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Course also available customized

Next sessions, see : *http://www.mvd-fpga.com/en/formationsCalend.html*

TOPICS

ARCHITECTURE OF I.MX27

- ARM core based architecture
- Clarifying the internal data paths
- Highlighting the purpose of the 2 central interconnect units : MAX and M3IF
- Organization of a board based on i.MX27
- Mapping

THE ARM926EJ-S CORE

- Presentation of the core
- Operating modes
- Pipeline
- ARM vs Thumb instruction sets, interworking
- Branch instructions
- C-to-Assembly interface
- Exception mechanism
- Debug facilities

RESET AND CLOCKING

- Clock distribution
- Power-up sequence
- Low power modes, clock gating
- System boot mode selection
- Bootstrap mode operation

SYSTEM CONTROL

- GPIO module
- General Purpose Input interrupt request capability
- Signal description

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DMA CONTROLLER

- Channel priority definition
- Burst length definition
- 2D memory transfers
- Double-buffering mechanism enabling chained transfers

ACCESSING EXTERNAL MEMORIES

- Description of the Master Arbitration and Buffering [MAB] unit
- Description of the M3IF arbitration [M3A]
- Enhanced DDR SDRAM controller
- NAND flash controller, boot from flash
- Programming the chip-selects

STANDARD PARALLEL INTERFACES

ATA CONTROLLER

- PIO mode
- Ultra DMA mode
- FIFO receive and FIFO transmit alarms

MSHC

- Transfer protocol
- Error management

SDHC

- Interface to SD cards
- Transfer protocol
- Error management

VIDEO PROCESSING UNITS

VIDEO ACQUISITION

- CSI interface
- Configuring the interface to support CCIR656

VIDEO PRE-PROCESSOR

- Image resizing
- Color space conversion

VIDEO POST-PROCESSOR

- Deblock
- Dering
- Image resizing
- Color space conversion

VIDEO CODEC

- MPEG-4 encoding / decoding
- H.264 AVC encoding / decoding

AUDIO RELATED INTERFACES

SSI INTERFACES

- Connection of Codecs or DSPs
- AC97 support

DIGITAL AUDIO MULTIPLEXOR

- Connecting host interfaces to peripheral interfaces
- Internal network mode

SECURITY MODULES

SECURITY CONTROLLER

SAHARA2 SECURITY COPROCESSOR

- Random number generator
- Encryption / decryption sequences

RUN-TIME INTEGRITY CHECKER

- SHA-1 message authentication
- Segmented data gathering

IC IDENTIFICATION MODULE

COMMUNICATION CONTROLLERS

1-WIRE INTERFACE

CONFIGURABLE SPI

- SPI protocol basics
- Master / slave operation
- Transfer sequence

I2C INTERFACES

- I2C protocol basics
- Master vs slave
- Transfer sequence

UART

- IrDA modulation / demodulation
- Support for Smart Card
- Flow control

USB

- Explaining what is OTG
- High-speed operation
- EHCI support
- Full speed operation
- Endpoint configuration

FAST ETHERNET CONTROLLER [FEC]

- Buffer management, based on Buffer Descriptors
- Incoming frame filtering mechanisms
- VLAN support

LCD CONTROL

LCDC

- LCD screen format
- Standard panel interface for common LCD drivers
- Graphic window on screen

SLCDC

- Interface to an external display controller
- Transferring images and controls from DDR to the external controller

GENERATING THE LINUX KERNEL IMAGE

- What is required on the host before installing LTIB
- Common package selection screen
- Common target system configuration screen
- Building a complete BSP with the default configurations
- Creating a Root Filesystems image
- Re-configuring the kernel under LTIB
- Selecting user-space packages
- Setup the bootloader arguments to use the exported RFS
- Debugging Uboot and the kernel by using Trace32
- Adding a new package
- Other deployment methods
- Creating a new package and integrating it into LTIB

DOCUMENTATION

Training manuals will be given to attendees during training in print.