

i.MX31 IMPLEMENTATION + LTIB

Ref : 004732A

Duration : 4 days

OBJECTIVES

- The course details the hardware implementation of the i.MX31 microcontroller
- The boot sequence and the clocking are explained
- The course explains all parameters that affect the performance of the system in order to easily perform the final tuning
- A description of all internal peripherals is provided
- An overview of the ARM1136 core helps to understand issues caused by cache and MMU
- The course ends with practical labs explaining how to generate a Linux image as well as a Root File System, by using a tool called LTIB [Linux Target Image Builder]

RELATED COURSES

- USB training (Ref.002606A)
- CAN training (Ref.002601A)
- Ethernet training (Ref.003367A)
- ARM1136 System Design (Ref.004802A)

PARTNERS

- MVD Training is a Freescale Alliance Member
- MVD Training's Freescale related courses are approved by Freescale

PREREQUISITES

- A basic understanding of microprocessors and microcontrollers is recommended
- A basic understanding of digital logic or hardware / ASIC design issues would be useful but not essential
- A basic understanding of assembler or C programming would be useful but not essential



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Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

ARCHITECTURE OF i.MX31

- Clarifying the internal data paths : AHB bus, peripheral buses
- Highlighting the purpose of the 2 central interconnect units : MAX and M3IF
- Organization of a board based on i.MX31

THE ARM1136JF-S CORE

- Presentation of the core, architecture and programming model
- Operating modes : user, system, super, IRQ, FIQ, undef and abort
- ARM vs Thumb instruction sets, interworking
- Branch instructions, implementation of C call and return statements
- Level1 cache operation
- Memory management unit
- C-to-Assembly interface
- Exception mechanism, handler table
- Debug facilities

RESET AND CLOCKING

- Clock distribution
- PLL output frequency calculation
- Power-up sequence
- Low power modes, clock gating
- Global reset vs warm reset
- System boot mode selection

SYSTEM CONTROL

- GPIO module
- General Purpose Input interrupt request capability
- Signal description

THE ARM11 PLATFORM

- MAX parameterizing
- ARM Vector Interrupt Controller

- Level 2 cache operation

SMART DMA CONTROLLER

- Scheduler
- CRC calculation unit
- SDMA initialisation
- Instruction description

ACCESSING EXTERNAL MEMORIES

- Description of the Master Arbitration and Buffering [MAB] unit
- Description of the M3IF arbitration [M3A]
- Introduction to DDR SDRAM
- Enhanced DDR SDRAM controller
- NAND flash controller, boot from flash

STANDARD PARALLEL INTERFACES

- ATA controller
- MSHC
- SDHC

VIDEO PROCESSING UNITS

- Video acquisition
- MPEG4 encoder
- Image Processing Unit
- Graphics accelerator

AUDIO RELATED INTERFACES

- SSI interfaces
- Digital audio multiplexer

COMMUNICATION CONTROLLERS

- 1-wire interface
- Configurable SPI
- I2C interfaces
- UART
- USB

GENERATING THE LINUX KERNEL IMAGE

- Introducing the tools required to generate the kernel image
- What is required on the host before installing LTIB
- Common package selection screen
- Common target system configuration screen
- Building a complete BSP with the default configurations
- Creating a Root Filesystems image
- Re-configuring the kernel under LTIB
- Selecting user-space packages
- Setup the bootloader arguments to use the exported RFS
- Debugging Uboot and the kernel by using Trace32
- Command line options
- Adding a new package
- Other deployment methods
- Creating a new package and integrating it into LTIB
- A lot of labs have been created to explain the usage of LTIB

DOCUMENTATION

Training manuals will be given to attendees during training in print.