

AT91RM9200 MICROCONTROLLERS IMPLEMENTATION

Ref : 004749A

Duration : 4 days

OBJECTIVES

- The course details the hardware implementation of the AT91RM9000
- The ARM920T operation is detailed, particularly cache and MMU
- The boot sequence and the clocking are explained
- Practical labs on integrated peripherals are based on I/O functions provided by Atmel
- The course provides examples of internal peripheral software drivers

RELATED COURSES

- USB training (Ref.002606A)
- CAN training (Ref.002601A)
- Ethernet training (Ref.003367A)
- ARM-7 / ARM-9 System Design (Ref.002879A)
- ARM Software development using RealView (Ref.002580A)

PARTNERS

- This training is referenced by ATMEL

PREREQUISITES

- A basic understanding of microprocessors and microcontrollers is recommended
- A basic understanding of digital logic or hardware / ASIC design issues would be useful but not essential
- A basic understanding of assembler or C programming would be useful but not essential

PRACTICAL LABS

- For on-site courses, labs can be run under the following environments : Keil μ Vision, or IAR Workbench
- For open courses, labs are run under IAR Workbench



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Course also available
 customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

INTRODUCTION TO AT91RM9200 [1-hour]

- ARM core based architecture, AMBA buses
- APB internal busses
- The main three blocks : platform, core and input / output peripherals

THE ARM920T CORE [11-hour]

- Presentation of the core, architecture and programming model
- Operating modes : user, system, super, IRQ, FIQ, undef and abort
- Pipeline, calculation of the CPI
- ALU data path
- ARM vs Thumb instruction sets, interworking
- Access to memory-mapped locations, addressing modes
- Write buffer
- Stack management
- Branch instructions, implementation of C call and return statements
- Benefits of condition set capability in ARM state
- C-to-Assembly interface
- Exception mechanism, handler table
- MMU, format of page descriptor tables
- Cache operation
- Assigning attributes and access rights to pages
- JTAG interface
- Debug facilities, 2-wire UART and support for debug communication channel interrupt

INFRASTRUCTURE [6-hour]

- Power supplies, internal regulator
- Power-on sequence
- Clock generator, on-chip oscillator, PLL
- Reset controller based on Power-on reset cells and low-power factory-calibrated brownout detector
- Boot program

- External reset
- Memory controller, embedded flash controller, memory protection unit, abort status and misalignment detection
- Internal high-speed flash, prefetch buffer, sector lock capability, flash security bit
- External Bus Interface, SDRAM controller, NAND flash controller
- Power management controller, slow clock mode, idle mode, 3 programmable external clock signals
- Advanced interrupt controller
- Individually maskable, 8-level priority, vectored interrupt sources
- External interrupt sources and fast interrupt source
- Parallel input / output controller, programming the pin multiplexers, input change capability interrupt
- 4 high-current drive I/O lines
- Peripheral DMA controller

TIMERS [2-hour]

- Periodic Interval Timer
- Windowed Watchdog
- Real-time timer
- 3-channel timer / counter, double PWM generation, capture / waveform mode, up/down capability

COMMUNICATION CONTROLLERS [10-hour]

2-wire interface

- I2C protocol basics
- Slave mode vs master mode
- Transmit and receive sequences

SPI

- SPI protocol basics
- Master / slave operation
- External chip-select
- Transfer sequence

USART

- Individual baud rate generators
- IrDA modulation / demodulation
- Support for Smart Card
- RS485 support
- Flow control
- Practical lab : Communication with a PC, using HyperTerminal

Synchronous Serial Controller

- Independent clock and frame sync signals for each receiver and transmitter
- I2S analog interface support
- Time Division Multiplexed support
- High speed continuous data stream capabilities

Ethernet MAC

- Full duplex vs half duplex operation
- Accessing PHY registers, auto-negotiation
- Receive and Transmit buffer management, buffer descriptors
- Incoming frame filtering
- Error management

- Practical lab : Communication with a PC, using Wireshark

USB device

- Full speed operation
- Endpoint configuration

USB host

- Overview of the OHCI specification
- Understanding how USB packets are prepared and scheduled for transmission, transfer descriptor
- Clarifying the boundary between software and hardware

Multimedia Card Interface (on demand)

- MMC and SD card basics
- Hardware interface
- Command / response protocol
- Read sequence
- Write sequence
- Related interrupts

DOCUMENTATION

Training manuals will be given to attendees during training in print.