AT91SAM9 MICROCONTROLLERS IMPLEMENTATION

Ref : 004761A **Duration : 4 days**

OBJECTIVES

- The course details the hardware implementation of the AT91SAM9 MCUs
- The ARM926EJ-S operation is detailed, particularly cache and MMU
- The boot sequence and the clocking are explained
- Practical labs on integrated peripherals are based on I/O functions provided by Atmel
- The course provides examples of internal peripheral software drivers

RELATED COURSES

- USB training (Ref.002606A)
- CAN training (Ref.002601A)
- ARM-7 / ARM-9 System Design (Ref.002879A)
- ARM Software development using RealView (Ref.002580A)

PARTNERS

- This training is referenced by ATMEL

PREREQUISITES

- A basic understanding of microprocessors and microcontrollers is recommended
- A basic understanding of digital logic or hardware / ASIC design issues would be useful but not essential
- A basic understanding of assembler or C programming would be useful but not essential

PRACTICAL LABS

- For on-site courses, labs can be run under the following environments : Keil µVision, or IAR Workbench
- For open courses, labs are run under IAR Workbench

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Course also available customized

Next sessions, see : *http://www.mvd-fpga.com/en/formationsCalend.html*

TOPICS

INTRODUCTION TO AT91SAM9 MCUs [1-hour]

- ARM core based architecture, AMBA buses
- Multi-layer AHB bus matrix
- APB internal busses
- The main three blocks : platform, core and input / output peripherals

THE ARM926EJ-S CORE [11-hour]

- Presentation of the core, architecture and programming model
- Operating modes : user, system, super, IRQ, FIQ, undef and abort
- Pipeline, calculation of the CPI
- ALU data path
- ARM vs Thumb instruction sets, interworking
- Access to memory-mapped locations, addressing modes
- Write buffer
- Stack management
- Branch instructions, implementation of C call and return statements
- Benefits of condition set capability in ARM state
- C-to-Assembly interface
- Exception mechanism, handler table
- MMU, format of page descriptor tables
- Fast Context Switch Extension
- Cache operation, replacement policy, locking
- Using CP15 instructions to control cache and MMU
- Assigning attributes and access rights to pages
- JTAG interface
- Debug facilities

INFRASTRUCTURE [6-hour]

- Power supplies, internal regulator
- Power-on sequence
- Clock generator, on-chip oscillator, PLL
- Reset controller based on Power-on reset cells and low-power factory-calibrated brownout detector
- Boot program
- External reset
- Memory controller, embedded flash controller, memory protection unit, abort status and misalignment detection
- Internal high-speed flash, prefetch buffer, sector lock capability, flash security bit
- External Bus Interface, SDRAM controller, NAND flash controller
- Power management controller, slow clock mode, idle mode, 3 programmable external clock signals
- Advanced interrupt controller
- Individually maskable, 8-level priority, vectored interrupt sources
- External interrupt sources and fast interrupt source
- Parallel input / output controller, programming the pin multiplexers, input change capability interrupt
- Peripheral DMA controller

TIMERS [1-hour]

- Periodic Interval Timer
- Windowed Watchdog
- Real-time timer
- 3-channel timer / counter, double PWM generation, capture / waveform mode, up/down capability

ANALOG-TO-DIGITAL CONVERTER [1-hour]

- Successive Approximation Register 10-bit ADC
- Detail of the analog part, timings
- Conversion triggers
- Related interrupts

COMMUNICATION CONTROLLERS [10-hour]

2-WIRE INTERFACE

- I2C protocol basics
- Slave mode vs master mode

- Transmit and receive sequences

SPI

- SPI protocol basics
- Master / slave operation
- External chip-select
- Transfer sequence

USART

- Individual baud rate generators
- IrDA modulation / demodulation
- Support for Smart Card
- RS485 support
- Flow control
- Practical lab : Communication with a PC, using HyperTerminal

SYNCHRONOUS SERIAL CONTROLLER

- Independent clock and frame sync signals for each receiver and transmitter
- I2S analog interface support
- Time Division Multiplexed support
- High speed continuous data stream capabilities

ETHERNET MAC

- Full duplex vs half duplex operation
- Accessing PHY registers, auto-negotiation
- Receive and Transmit buffer management, buffer descriptors
- Incoming frame filtering
- Error management
- Practical lab : Communication with a PC, using Wireshark

USB DEVICE

- Full speed operation
- Endpoint configuration
- High Speed device port on AT91SAM9RL64
- Connection of an external PHY using UTMI+

USB HOST

- Overview of the OHCI specification
- Understanding how USB packets are prepared and scheduled for transmission, transfer descriptor
- Clarifying the boundary between software and hardware

MULTIMEDIA CARD INTERFACE (ON DEMAND)

- MMC and SD card basics
- Hardware interface
- Command / response protocol
- Read sequence
- Write sequence
- Related interrupts

AC97 CONTROLLER (SPECIFIC TO AT91SAM9RL64, ON DEMAND)

- Sound encoding
- Connecting an external audio codec
- Time slot assigner operation

IMAGE SENSOR INTERFACE [Specific to AT91SAM9XE128/256/512, on demand]

- Connecting an external image sensor
- CCIR656 specification
- Horizontal and Vertical synchronization
- Scaling, decimation
- Colour space conversion
- FIFO and DMA transfer

LCD CONTROLLER [Specific to AT91SAM9RL64, on demand]

- Single and Dual scan colour and monochrome passive STN LCD panels
- Single scan active TFT LCD panels
- Pixel encoding
- Supported resolution

TOUCH SCREEN ANALOG-TO-DIGITAL CONVERTER [Specific to AT91SAM9RL64, on demand]

- 6-channel ADC
- 4-wire resistive touch screen
- Multiple trigger sources
- Conversion sequencer

DOCUMENTATION

Training manuals will be given to attendees during training in print.