
ARM1136 SYSTEM DESIGN

Ref : 004802A

Duration : 4 days

OBJECTIVES

- This course takes an **in depth** look at the considerations you will need to take into account when designing a system containing an ARM1136 core
- **It is aimed at :**
 - Software engineers who not only want to obtain details of how to write software to run on the ARM11, but also wish to obtain an understanding of hardware design issues
 - Hardware engineers who need to understand how to design ARM11 based systems, but also wish to obtain an understanding of the issues of writing software to run on that system

RELATED COURSES

- ARM-7 / ARM-9 System Design (Ref.002879A)

PARTNERS

- This training course is approved by ARM

PREREQUISITES

- A basic awareness of the ARM is highly recommended especially the knowledge of ARM V4T and V5TE architectures
- A basic understanding of microprocessors and microcontrollers is recommended
- A basic understanding of digital logic or hardware / ASIC design issues would be useful but not essential
- A basic understanding of assembler or C programming would be useful but not essential
- A basic awareness ARM cores is useful but not essential

PRACTICAL LABS

- For on-site courses, labs can be run under the following environments : CodeWarrior/ADS/AXD, Eclipse/RVDS, Keil μ Vision, GNU/Lauterbach simulator, or IAR Workbench
- For open courses, labs are run under Eclipse/RVDS



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Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

First day

THE ARM ARCHITECTURE

- ARM operation modes
- The ARM registers set, register organization summary according to the current mode
- Program Status Registers
- Exception handling, vector table, automatic switch into ARM mode
- Instruction sets

ARM11 CPU ARCHITECTURE

- ARM11 superscalar pipeline operation
- Dynamic vs static branch prediction
- Out of order execution
- Return stack

ARM1136 OVERVIEW

- Block diagram
- AXI (AMBA3) interfaces
- ARM1176 example system
- Reset and clocking
- Booting

MEMORY SUBSYSTEMS

- Cache basics
- Hit under miss and its consequence : out of order abort
- ARM11 related instructions
- Highlighting data flows between main memory, L1 cache and L2 cache
- Tightly coupled memories

- Configuration & control through CP15

Second day

MEMORY MANAGEMENT & PROTECTION

- Introduction to page management
- V6 virtual memory architecture
- ARM V6 endianness
- Data alignment
- Memory Barriers

ARMv6 INSTRUCTION SET

- Additional classes of instruction
- Standard multiply extension
- Long multiplication
- Packed data types
- V6z NOP32 instruction to enter low power mode

PRIMECELL VECTORED INTERRUPT CONTROLLER

- Interrupt controllers
- Primecell VICs
- Reducing interrupt latency through automatic vector generation
- VIC basic signal timing
- Interrupt priority and masking

Third day

AHB PROTOCOL

- Transfers with AHB
- Use of HREADY, HRESP & HTRANS signals

- Implementation of indivisible transactions

AXI PROTOCOL

- Topology : direct connection, multi-master, multi-layer
- PL300 AXI interconnect
- AXI channels, channel handshake
- Support for unaligned data transfers
- Transaction ordering, out of order transaction completion
- Read and write burst timing diagrams

APB

- Address decoding stages
- APB interconnect
- APB in AMBA3

ARM11 DEBUG

- Basic debug requirements
- Embedded core debug
- DBGAP interfacing

TRACING AN ARM11-BASED SYSTEM

- Motivation to real-time trace
- About core sight ETM11

- Tracing with core sight ETM11
- Implementing trace : ETB

Fourth day

LEVEL ONE AND LEVEL TWO MEMORY SYSTEMS

- TCM and cache interaction
- DMA channel
- Endianness
- Peripheral interface transfers
- AHB ports
- Implementation of the L210 level-2 cache controller

ARM11 MULTI-PROCESSOR SYNCHRONISATION

- Introduction to semaphore
- Using the SWP instruction
- Using ARMv6 synchronisation instructions : LDREX, STREX and CLREX

INTELLIGENT ENERGY MANAGER

- Conventional power management

DOCUMENTATION

Training manuals will be given to attendees during training in print.