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## PPC 464 CORE

Ref : 004804A

Duration : 3 days

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### OBJECTIVES

- A boot firmware that initializes the MMU has been developed
- Internal debug facilities are described
- The course focuses on PPC464 low level programming, especially the PowerPC EABI
- Examples of exception handlers are provided
- A DFT has been developed to explain how to use MAC instructions
- The Floating Point Unit operation is described

### RELATED COURSES

- The knowledge of C language for real-time and embedded applications (course 002603A) is recommended
- In order to understand how the core communicates with peripherals, the CoreConnect course (reference 002585A) is also recommended

### PREREQUISITES

- Experience of a 32 bit processor or DSP is mandatory

### PARTNERS

- This training course is approved by IBM microelectronics

### Contact

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Course also available  
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

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### TOPICS

#### INTRODUCTION TO PPC464FP-H90

- Internal architecture overview
- Highlighting instruction and data paths
- Clocking
- Programming model, the 4 register groups GPRs, SPRs, DCRs and memory mapped
- CoreConnect-based SOCs

#### THE CORE ARCHITECTURE

- Pipeline basics
- 7-stage pipeline operation
- Speculative execution, guarded memory
- Serialization
- Cache basics
- Cache programming interface
- Process vs thread
- Memory Management Unit
- 36-bit real address space
- Translation Lookaside Buffer initialisation
- Cache control and debugging features
- Load / store buffer, speculative loads, msync and mbar instructions

#### BOOK E COMPLIANT CORE

- Booke E objectives
- Branch instructions
- Addressing modes
- Load / store instructions
- Semaphore management with lwarx / stwxc. Instructions
- Arithmetical and logical instructions, shift and rotate instructions

- Floating point unit, compliancy with IEEE754
- Processing denormalized FP numbers
- Floating point arithmetic instructions
- FP-to-integer and integer-to-FP casting
- The PowerPC EABI
- Cache related instructions
- 16-bit mac instructions to develop fixed point DSP algorithms
- 2-cycle multiply option
- Exception processing
- Critical versus non critical interrupts
- Syndrome registers updating when an exception is taken
- Core timers : PIT, FIT and WDT

#### INTEGRATED DEBUG FACILITIES

- JTAG emulator use
- The 464 instruction trace port
- Real time trace when the PowerPC core executes cached instructions
- Hardware vs software breakpoints

#### HARDWARE IMPLEMENTATION OF THE PPC464 CORE

- Signal naming convention
- External connections
- Clock and power management interface
- CPU control interface
- Reset interface
- External interrupt controller interface
- Instruction-side PLB interface
- Data-side PLB interface
- DCR interface

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### DOCUMENTATION

Training manuals will be given to attendees during training **both in pdf and in print**. Precise and easy to use, those notes can be used as a reference afterwards.

### CONTACT INFORMATIONS

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