
PPC440 and CrossBar,Virtex5-FXT

Ref : 004839A

Duration : 3 days

OBJECTIVES

- Learn the PPC440 core improvement with practical examples
- PPC405 compatibility and limits of StandAlone design
- Details about PPC440 core especially Cache management, MMU, pipeline and exceptions management
- PPC440 connections : PLB, APU and DCR
- Learn the CrossBar functionalities
- Reset and Clock circuitry
- LocalLink usage and associated DMA
- Give Architecture examples easily done using EDK

RELATED COURSES

- Virtex PowerPC system Implementation (002952A)

PARTNERS

- This training course is approved by XILINX

PREREQUISITES

- Good experiment using EDK tool

TRAINING MATERIALS

Software Configuration :

- Xilinx ISE Design Suite 11.3 Embedded Edition

Recommended Hardware Configuration :

- Intel Core 2 or equivalent
- Windows XP
- 1 GB Free disk after software installation
- At least 1Go RAM
- Minimum Display resolution : 1024 x 768
- On Site training : video projector

 **Authorized Training Provider**

Contact

Tel : 05 62 13 52 32
Fax : 05 61 06 72 60
training@mvd-fpga.com

Course also available
customized

Next sessions, see : <http://www.mvd-training.com/en/schedule.html>

TOPICS

Introduction

Instruction Pipeline

- 7 levels, superscalar
- branch management
- Synchronization
- Software support

Cache units

- 64 ways associative cache
- Normal, transitory or locked way
- Software support

MMU

- Overview
- Structure and attributes
- Software support

CrossBar

- Overview
- Arbiter
- Address decoding
- Buffer and transfers
- Software support

Load/Store Buffer

- Synchronization
- Software support

Exceptions management

- Mechanism
- Timer and WatchDog
- Handler Table

Clock and Reset

- Clock and alignments
- Clock generator block
- Reset signals and timing constraints
- Reset generator Block

Debug

- Software or Hardware Breakpoints
- Advanced breakpoints
- Software support

DCR interface

- Indirect addressing
- External Master
- Software support

PLB 4.6 implementation

- Overview
- IP creation

LocalLink and DMA

- Signals and protocol
- DMA operations
- IP creation
- Software support

Memory controller interface

- Signals and protocol
- Memory controller blocs

APU

- Overview
- FPU block

DOCUMENTATION

Training manuals will be given to attendees during training in print.