
DSP design with AcceIDSP

Ref : 004850A

Duration : 2 days

OBJECTIVES

- Learn to synthesize an algorithm written in m language from Matlab to a Xilinx FPGA Design using AcceIDSP synthesize tool.
- Transform a non synthesizable m code to synthesizable one.
- Quantization : specification and analyze of results.
- Modify a FIR filter to a polyphase decimator FIR filter synthesizable.
- Add control to your design
- Merge the synthesized result into a larger HDL design or into a SystemGenerator design

RELATED COURSES

- DSP design with System Generator (002836A)
- DSP implementation techniques for Xilinx FPGAs (002838A)

PARTNERS

- This training course is approved by XILINX

PREREQUISITES

- Good knowledge of Mathworks Matlab and .m coding
- Basic knowledge of digital signal Processing
- Knowledge of DSP resources inside Xilinx FPGAs
- Basic knowledge of the System Generator tool

TRAINING MATERIALS

Software Configuration :

- Xilinx ISE 10.1 SP3 + IP Update 3 + ISIM
- System Generator for DSP 10.1 SP3
- AcceIDSP 10.1 SP3
- Matlab 2007b or 2008a

Recommended Hardware Configuration :

- Intel Core 2 or equivalent
- Windows XP
- 1 GB Free disk after software installation
- At least 1Go RAM
- Minimum Display resolution : 1024 x 768
- On Site training : video projector



Contact

Tel : 05 62 13 52 32
Fax : 05 61 06 72 60
training@mvd-fpga.com

Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

1st day

- Introduction to the AcceIDSP Synthesis Tool
 - lab
- Synthesizable MATLAB Software design
 - lab
- Quantization
 - lab
- Multirate Design
 - lab
- Using AcceWare reference designs
 - Lab

2nd day

- Design exploration
 - Lab
- Adding hardware control
 - Lab
- Coding for hardware performance and efficiency
 - Lab
- Synthesizing Complex Numbers
 - Lab
- Interfacing to System Hardware
 - Lab
- System Generator Integration
 - Lab

DOCUMENTATION

Training manuals will be given to attendees during training in print.